KEITHLEY

Model 82-WIN Simultaneous C-V Measurement

User's Manual

A GREATER MEASURE OF CONFIDENCE

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Keithley Instruments, Inc. warrants the following items for 90 days from the date of shipment: probes, cables, rechargeable batteries, diskettes, and documentation.

During the warranty period, we will, at our option, either repair or replace any product that proves to be defective.

To exercise this warranty, write or call your local Keithley representative, or contact Keithley headquarters in Cleveland, Ohio. You will be given prompt assistance and return instructions. Send the product, transportation prepaid, to the indicated service facility. Repairs will be made and the product returned, transportation prepaid. Repaired or replaced products are warranted for the balance of the original warranty period, or at least 90 days.

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Manual Print History

The print history shown below lists the printing dates of all Revisions and Addenda created for this manual. The Revision Level letter increases alphabetically as the manual undergoes subsequent updates. Addenda, which are released between Revisions, contain important change information that the user should incorporate immediately into the manual. Addenda are numbered sequentially. When a new Revision is created, all Addenda associated with the previous Revision of the manual are incorporated into the new Revision of the manual. Each new Revision includes a revised copy of this print history page.

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KEITHLEY Safety Precautions

The following safety precautions should be observed before using this product and any associated instrumentation. Although some instruments and accessories would normally be used with non-hazardous voltages, there are situations where hazardous conditions may be present.

This product is intended for use by qualified personnel who recognize shock hazards and are familiar with the safety precautions required to avoid possible injury. Read and follow all installation, operation, and maintenance information carefully before using the product. Refer to the manual for complete product specifications.

If the product is used in a manner not specified, the protection provided by the product may be impaired.

The types of product users are:

Responsible body is the individual or group responsible for the use and maintenance of equipment, for ensuring that the equipment is operated within its specifications and operating limits, and for ensuring that operators are adequately trained.

Operators use the product for its intended function. They must be trained in electrical safety procedures and proper use of the instrument. They must be protected from electric shock and contact with hazardous live circuits.

Maintenance personnel perform routine procedures on the product to keep it operating properly, for example, setting the line voltage or replacing consumable materials. Maintenance procedures are described in the manual. The procedures explicitly state if the operator may perform them. Otherwise, they should be performed only by service personnel.

Service personnel are trained to work on live circuits, and perform safe installations and repairs of products. Only properly trained service personnel may perform installation and service procedures.

Keithley products are designed for use with electrical signals that are rated Installation Category I and Installation Category II, as described in the International Electrotechnical Commission (IEC) Standard IEC 60664. Most measurement, control, and data I/O signals are Installation Category I and must not be directly connected to mains voltage or to voltage sources with high transient over-voltages. Installation Category II connections require protection for high transient over-voltages often associated with local AC mains connections. Assume all measurement, control, and data I/O connections are for connection to Category I sources unless otherwise marked or described in the Manual.

Exercise extreme caution when a shock hazard is present. Lethal voltage may be present on cable connector jacks or test fixtures. The American National Standards Institute (ANSI) states that a shock hazard exists when voltage levels greater than 30V RMS, 42.4V peak, or 60VDC are present. **A good safety practice is to expect that hazardous voltage is present in any unknown circuit before measuring.**

Operators of this product must be protected from electric shock at all times. The responsible body must ensure that operators are prevented access and/or insulated from every connection point. In some cases, connections must be exposed to potential human contact. Product operators in these circumstances must be trained to protect themselves from the risk of electric shock. If the circuit is capable of operating at or above 1000 volts, **no conductive part of the circuit may be exposed.**

Do not connect switching cards directly to unlimited power circuits. They are intended to be used with impedance limited sources. NEVER connect switching cards directly to AC mains. When connecting sources to switching cards, install protective devices to limit fault current and voltage to the card.

Before operating an instrument, make sure the line cord is connected to a properly grounded power receptacle. Inspect the connecting cables, test leads, and jumpers for possible wear, cracks, or breaks before each use.

When installing equipment where access to the main power cord is restricted, such as rack mounting, a separate main input power disconnect device must be provided, in close proximity to the equipment and within easy reach of the operator.

For maximum safety, do not touch the product, test cables, or any other instruments while power is applied to the circuit under test. ALWAYS remove power from the entire test system and discharge any capacitors before: connecting or disconnecting ca-

bles or jumpers, installing or removing switching cards, or making internal changes, such as installing or removing jumpers.

Do not touch any object that could provide a current path to the common side of the circuit under test or power line (earth) ground. Always make measurements with dry hands while standing on a dry, insulated surface capable of withstanding the voltage being measured.

The instrument and accessories must be used in accordance with its specifications and operating instructions or the safety of the equipment may be impaired.

Do not exceed the maximum signal levels of the instruments and accessories, as defined in the specifications and operating information, and as shown on the instrument or test fixture panels, or switching card.

When fuses are used in a product, replace with same type and rating for continued protection against fire hazard.

Chassis connections must only be used as shield connections for measuring circuits, NOT as safety earth ground connections.

If you are using a test fixture, keep the lid closed while power is applied to the device under test. Safe operation requires the use of a lid interlock.

If  or  is present, connect it to safety earth ground using the wire recommended in the user documentation.

The  symbol on an instrument indicates that the user should refer to the operating instructions located in the manual.

The  symbol on an instrument shows that it can source or measure 1000 volts or more, including the combined effect of normal and common mode voltages. Use standard safety precautions to avoid personal contact with these voltages.

The **WARNING** heading in a manual explains dangers that might result in personal injury or death. Always read the associated information very carefully before performing the indicated procedure.

The **CAUTION** heading in a manual explains hazards that could damage the instrument. Such damage may invalidate the warranty.

Instrumentation and accessories shall not be connected to humans.

Before performing any maintenance, disconnect the line cord and all test cables.

To maintain protection from electric shock and fire, replacement components in mains circuits, including the power transformer, test leads, and input jacks, must be purchased from Keithley Instruments. Standard fuses, with applicable national safety approvals, may be used if the rating and type are the same. Other components that are not safety related may be purchased from other suppliers as long as they are equivalent to the original component. (Note that selected parts should be purchased only through Keithley Instruments to maintain accuracy and functionality of the product.) If you are unsure about the applicability of a replacement component, call a Keithley Instruments office for information.

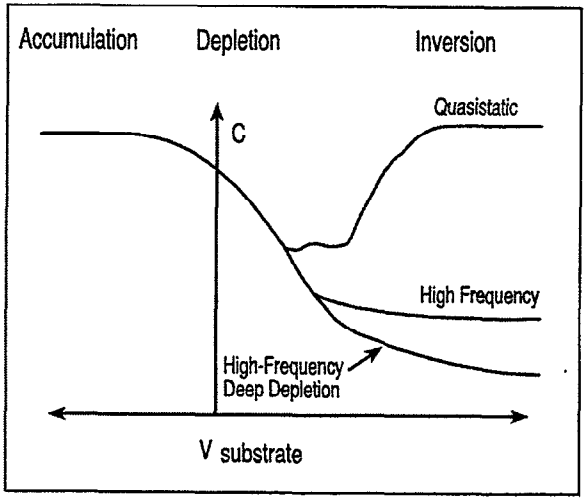
To clean an instrument, use a damp cloth or mild, water based cleaner. Clean the exterior of the instrument only. Do not apply cleaner directly to the instrument or allow liquids to enter or spill on the instrument. Products that consist of a circuit board with no case or chassis (e.g., data acquisition board for installation into a computer) should never require cleaning if handled according to instructions. If the board becomes contaminated and operation is affected, the board should be returned to the factory for proper cleaning/servicing.

User's Guide

Model 82-WIN Simultaneous C-V Measurement

Keithley Instruments, Inc.

Release Date: April 1997



Contents

C-V Measurement

Introduction

This chapter provides detailed information on using Metrics ICS software with Keithley Model 82-WIN to set up C-V measurements and acquire C-V data. A quicker and easier approach is to use Keithley libraries, which contain typical measurement setup parameters and analysis algorithms to extract many parameters from basic C-V measurements. The next chapter provides detailed information on how to use Keithley libraries.

This chapter is organized as the following:

Typical Measurement Sequence: Outlines the basic measurement sequence that should be followed to ensure accurate measurements and analysis.

First Time System Testing and Cable Correction: Describes the procedure to test the complete system for the presence of unwanted characteristics such as leakage resistance, leakage current, and stray capacitance. It also details the cable correction procedure that must be performed in order to ensure accuracy of high-frequency C-V measurement.

Measurement Procedures: Describes basic procedures for making C-V measurement. A simultaneous C-V measurement example is included to illustrate the procedures.

Choosing the Right Parameters: Briefly discusses the considerations in choosing right measurement parameters to achieve accurate C-V measurements. It also describes a procedure to determine the correct delay time to optimize C-V measurements.

Additional C-V Measurement Features: Includes a description of squarewave, single staircase, double staircase, and capacitance vs. delay time measurements.

Measurement Considerations: Outlines numerous factors that should be taken into account in order to maximize measurement accuracy and minimize errors.

Typical Measurement Sequence

Measurements should be carried out in the proper sequence in order to ensure that the system is optimized and error terms are minimized. The basic sequence is outlined below. If your system is properly set up, tested, and calibrated, you may skip Steps 1 and 2. Otherwise you must perform the testing and calibration procedures.

Step 1: Test and Correct for System Leakage and Strays

Initially, you should test and determine if any problems, such as excessive leakage or unwanted stray capacitance, are present. You should correct these problems before making C-V a measurement. Refer to your system manuals for proper installation and testing procedures. After initial testing, the system need be tested only when you have changed some aspects of its configuration, such as connecting cables or test fixtures.

Probe-up suppression should be performed before each measurement to ensure accuracy. This procedure is discussed in the measurement section in detail.

Step 2: Correct for Cabling Effects

Cable correction is necessary to compensate for transmission line effects through the connecting cables and remote input coupler. Transmission line effects are more significant at higher frequencies and with longer cables, or with switches in the system. Failure to perform cable correction will result in substantially reduced accuracy of high-frequency C-V measurement. In order to perform correction, you must connect the Model 5909 calibration capacitors to the system, and perform the correction procedure under Metrics ICS. Cable correction must be performed the first time you use your

system. After that, it needs to be performed only if the system configuration is changed in some manner, or if the ambient temperature changes by more than 5°C.

Step 3: Configure Your System with Metrics ICS

If you are not using the Keithley library setup to make C-V measurement, it will be necessary for you to properly configure your system under Metrics ICS, including GPIB, instrument, switching matrices, measurement parameters, etc. You should refer to the Metrics ICS and Keithley C-V Driver manuals for detailed information regarding configuration of your system.

Step 4: Make a C-V Measurement

Before you can actually make measurements, you must select measurement parameters such as sweep mode, range, frequency, and voltage values. As the sweep is performed, measured values are stored in data arrays for analysis and later retrieval.

Step 5: Analyze C-V Data

Besides Metrics ICS and Keithley C-V drivers, the Keithley C-V system includes libraries for setup and data analysis. Depending on the options you choose, you will be able to extract a large amount of useful information from your C-V measurement data. Available analysis features include doping profile, flatband capacitance and voltage, interface trap density, and mobile ion density, etc.

First Time System Testing and Cable Correction

Leakage Test

Before using the system, it is necessary to check system leakage. Zero suppress in Metrics ICS is intended to correct for small system leakage current and stray capacitance. Any excessive leakage problem must be solved before attempting a measurement. Procedures are outlined below.

You should run a probe-up test sweep to determine if there is excessive system or voltage-dependent leakage and stray capacitance. You may also load the Keithley standard system leakage check library. Refer to the *C-V Libraries and Analysis* chapter for information on using the leakage check library. Note that setup parameters should be same as those used for your measurement.

Once leakage check setup is loaded and properly configured, click on **Single** on the **Meas** button. After the sweep, you may view the capacitance and Q/t vs. voltage plots. There are two key items to note when performing this procedure. For a typical system, capacitance and Q/t values should be as small as possible. Ideally, the stray capacitance should be less than 1% of the expected capacitance values for optimal accuracy, and leakage current should be very small as well. Typically, leakage current should be less than 0.5 pA on the 200pF range, while on the 2nF range, leakage current should be less than 2pA. In addition, stray capacitance or leakage current should not display any voltage-dependent features.

Correcting for Excess Leakage Current

1. Make sure proper cables are installed in the correct places. Be certain you have not interchanged Model 4801 (low noise) cables with the Model 7051 (50Ω) cables or other regular cables.

2. Make sure all connecting jacks and connectors are free of contamination. Clean any dirty connectors with methanol, and allow them to dry thoroughly before use.

3. Be certain that you are making a probe-up measurement.

4. Check to see that no leakage paths are present in the test fixture.

5. If necessary, tie down cables to avoid noise currents caused by cable flexing. Also avoid vibration during testing.

Correcting for Stray Capacitance

1. Verify that all cables are of the proper type and not of excessive length.

2. Verify the integrity of all cable shields, and that the shield connections are carried through to the connectors.

3. Again, make sure the procedure is being performed in the probe-up configuration.

4. Use a test fixture of good, low capacitance design. Use low-noise, coaxial, or triaxial probes.

5. Make certain the test fixture shield is in place when characterizing the system. The same precaution holds true when characterizing or measuring a device.

6. If problems persist, see *Measurement Considerations* at the end of this chapter.

Cable Correction

The Keithley library disk includes a standard cable calibration file with typical cable compensation for the Keithley simultaneous C-V system; the file name is STANDARD.CAL. This file maybe be copied to the \ICS sub directory of the hard disk for initial use.

For optimal accuracy, system cables must be compensated, and you should perform a new cable calibration on your system. You may load the Keithley leakage check library for cable calibration purposes. Click on the **Setup Editor** button, then click on the **Opts** option button. If you have performed cable calibration, you may load the calibration file. Otherwise, you must perform cable calibration to assure measurement accuracy.

In order to perform cable calibration, you will need the Model 5909 calibration capacitors. Disconnect your test fixture and connect each calibration capacitor in its place when prompted to do so. Use the supplied female-to-female BNC adapters to connect the sources to the cables. Calibration capacitors should be connected to the end connecting to the probe station. When making the connection, be sure not to handle the cables and capacitors excessively, since the resulting temperature rise will change the capacitance values. Refer to Figure 1 for connections.

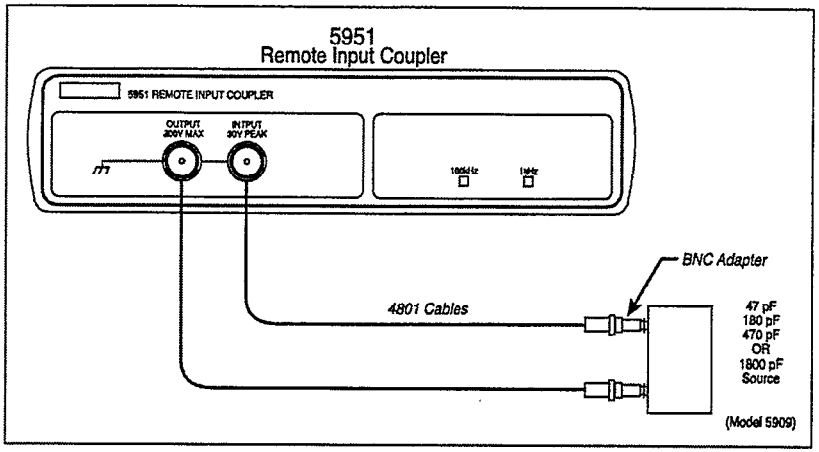


Figure 1 *Cable Correction Capacitor Connections*

Performing Cable Correction

1. Click on the **Calibration** button, and the cable calibration window shown in Figure 2 will be displayed.

2. Select the frequency and range you want to calibrate, then follow the prompts to connect the calibration capacitors to the cable.

3. Once calibration is finished, the screen should appear as shown in Figure 3.

4. Save this file as CABLE.CAL or the name you prefer. Note that the file extension must be .CAL.

5. Now load the calibration file, then exit the **Opts** window. You should now be in the **Setup** editor.

6. Click the **Done** button to exit Setup.

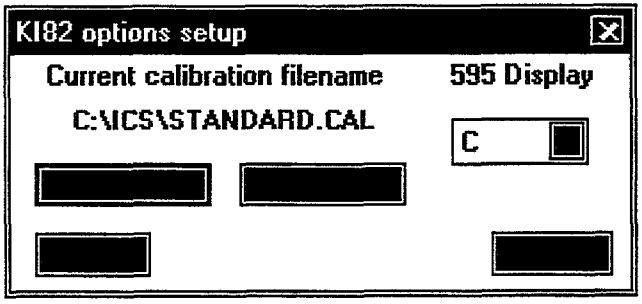


Figure 2 Options Setup Window

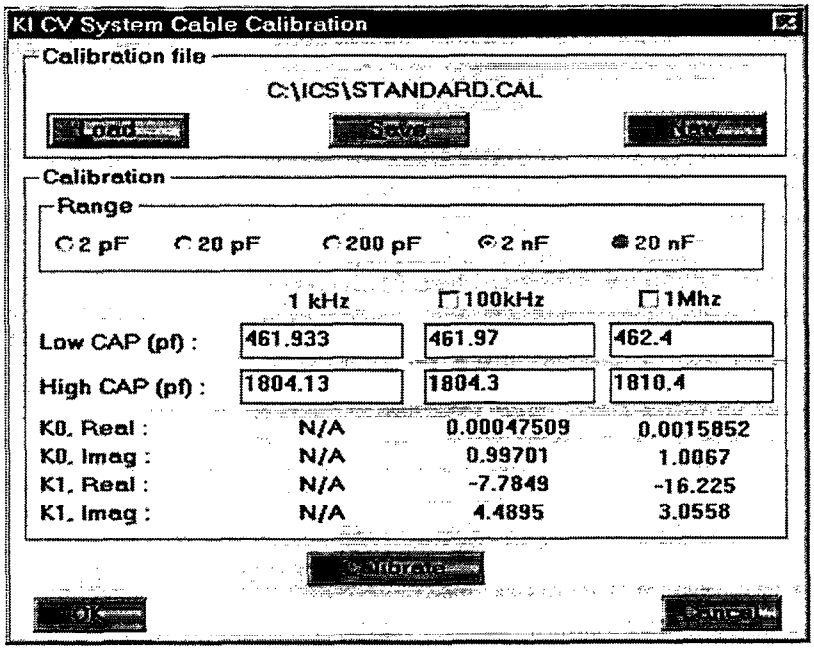


Figure 3 System Cable Calibration Window

Measurement Procedures

Detailed information about properly configuring your system can be found in Metrics ICS and Keithley Instruments C-V driver manuals. Here, only a brief summary related to Keithley C-V system is provided. An example of making a simultaneous C-V measurement is outlined.

GPIB Configuration

Once the GPIB board is properly installed and tested, click on the **GPIB** button on the menu strip. You should select the GPIB card installed in your computer (see Figure 4). Note that the GPIB Timeout option must be set to at least two times the expected maximum sweep delay time, or a GPIB timeout error may occur.

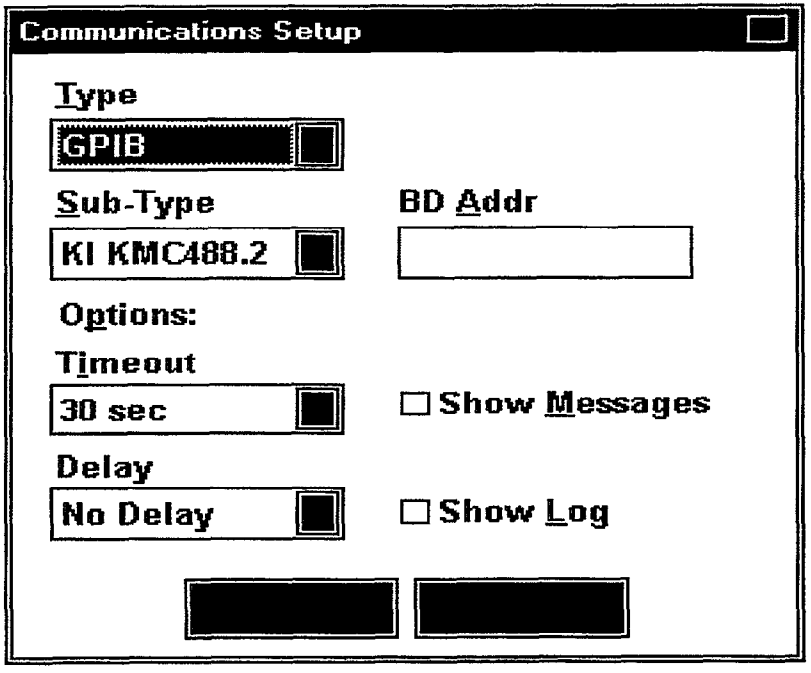


Figure 4 Communications Setup Window

Instrument Selection

You may have installed several Keithley instrument drivers with your Metrics core. You can make a selection here, such as a KI82 Simultaneous C-V system. Alternatively, you can select KI23x I-V, KI590 High Frequency C-V, and KI595 Quasistatic C-V instruments.

1. Click the **Connect** button to select the KI82 driver. The **GPIB** bus address menu appears when you click the **Configuration** button.

2. Type in the corresponding primary address for each instrument.

3. Click the **Verify** button to test if instruments are correctly configured. If they are not correctly configured, an error message will appear. Otherwise, the following message will be displayed: "The system is correctly configured."

4. Once the system is correctly configured, ICS will automatically store the configuration. After this procedure, the configuration step need not be run again unless the instrument configuration changes.

Instrument Setup

1. Click on the **Setup** button; the instrument setup editor window will appear. (See Figure 5.)

2. Click on **New**, and the program will prompt you to type in the Setup name.

3. Type in "Sim_CV," then click on the **Device** button. You may select many different devices. For this example, select the **MOSFET** icon.

4. Click on **Source Unit**, then click on **KI82 IN** to select the input.

5. Click on the **G** (gate) on the MOSFET symbol to connect the input to the gate.

6. Similarly, click on **KI82.OUT** to select the output, then click on the **B** (substrate) symbol of the MOSFET to connect the output to the substrate.

7. Click on the **KI82 OUT** icon; the measurement parameter setup window will appear. (See Figure 6.) You may now select the proper measurement parameters. The parameter window should appear like the one shown in the Figure 6. Refer to the Metrics ICS and Keithley C-V driver manuals for full details on all setup parameters.

8. Before you make a measurement, be sure to load the cable correction and calibration file. To do so, click on the **Opts**. button in the Setup Editor, then click on **Load** option to select the calibration file for your test fixture.

9. Exit from the **Opts.** window and the **Setup Editor** window.

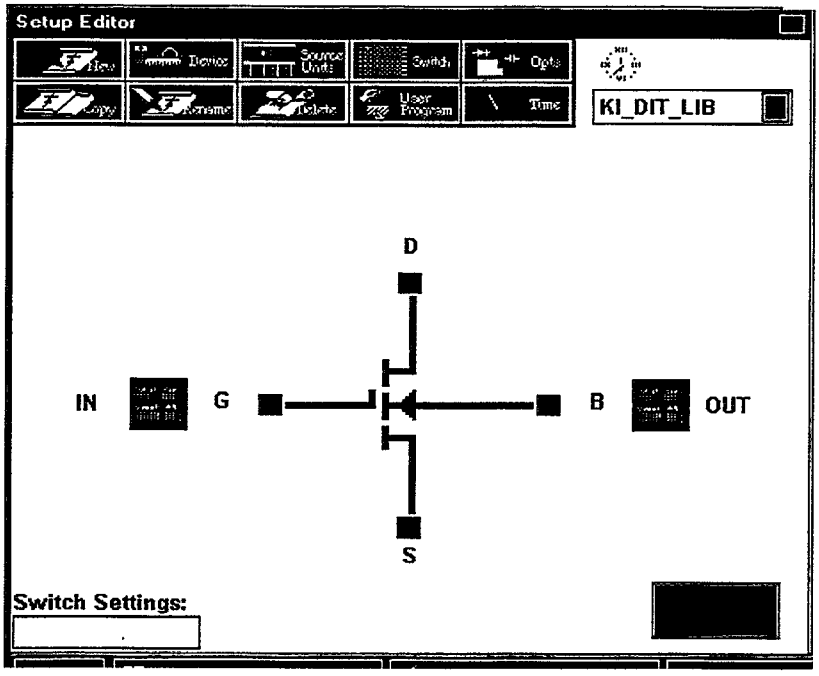


Figure 5 Instrument Setup Editor Window

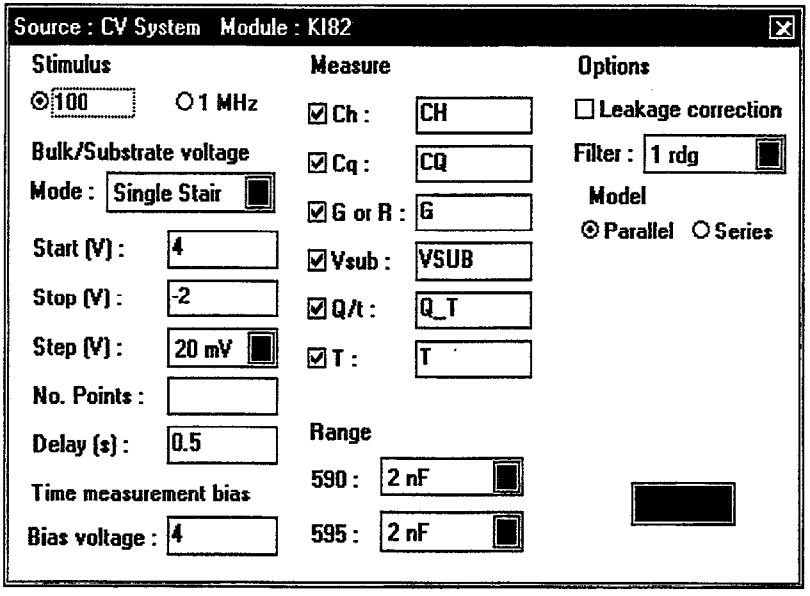


Figure 6 Measurement Setup Parameter Window

1. The zero cancel procedure described below will correct system leakage and stray capacitance. Note that large leakage current or stray capacitance should not be suppressed. Determine the source of the problems, and correct them before using your system.

2. Click on the **Meas.** button, and note there are several options from which to choose. (See Figure 7.)

3. Before you make measurements, you should do a probe-up zero suppress by clicking on the **Zero Cancel** button and following the instructions.

4. After the zero cancel procedure, the message "Please lower your probe" will be displayed on the screen. During this period, the Model 590 C-V meter is in its active reading mode, and you may lower your probe to contact the DUT while at same time observing the Model 590 display reading. Doing so ensures proper electrical contact between the probe and DUT.

5. You are now ready to make a C-V measurement. For this example, click on the **Single** button to make a single-sweep measurement. You may observe that when instrument finishes data taking, the data screen will flicker a few times. This situation is normal while ICS is updating the data. If the analysis package has been loaded, it make take some time to perform the calculations and display the data, depending on the amount of data and the speed of your computer.

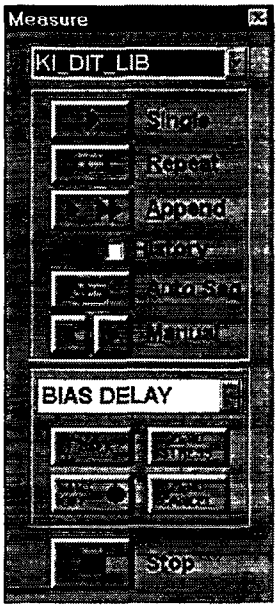


Figure 7 Measurement Selection Window

Analyzing Data

Before you attempt to analyze data, you should plot raw data and determine if there are any obvious measurement problems. Keep in mind that no analysis will compensate for substandard data caused by measurement problems. At this time, you may find it necessary to make a few adjustments to compensate for system-related problems and select better measurement parameters. If a large amount of noise is present, analysis results will not be dependable and may even be meaningless. Repeat the measurement procedure to determine the root cause of the problems, and correct them before proceeding.

1. The first step is to transfer the analysis constants to Metrics. Click on the **Transform Editor** button, then click on the **Edit Constants** button. You may type in the name, value, unit, and comments into the fields. These values are used in analysis.

2. Click on the **New Plot** button to draw a new graph. The **Setup Plot** window will pop up. (See Figure 8.)

3. Select the data option you wish to plot. For our example, select V_{SUB} as the **X-Axis** data parameter. For a simultaneous C-V measurement, plot both C_H and C_Q on the y-axis.

4. You may select one data set to plot on the y axis. Select the data you wish to plot on the **Y1-Axis** column. If you wish to plot another data set on a different scale but on the same graph, select that data set for the **Y2-Axis** column.

5. If you wish to plot two sets of data on the same scale you may use the **Build Group** feature. Click on the **Build Group** button, and add both C_H and C_Q to the group, for example Sim_CV. (See Figure 9.) After you close this window, you will notice a Sim_CV group is available under the y-axis sub-menu selection. Choose Sim_CV for the y-axis.

6. Click on **Apply** and then **Done**. You should see both C_Q and C_H curves plotted on the graph. By using the Build Group feature of Metrics ICS, you can put many curves on the same graph. Also notice that you can set up a second y-axis with different scale and different data set.

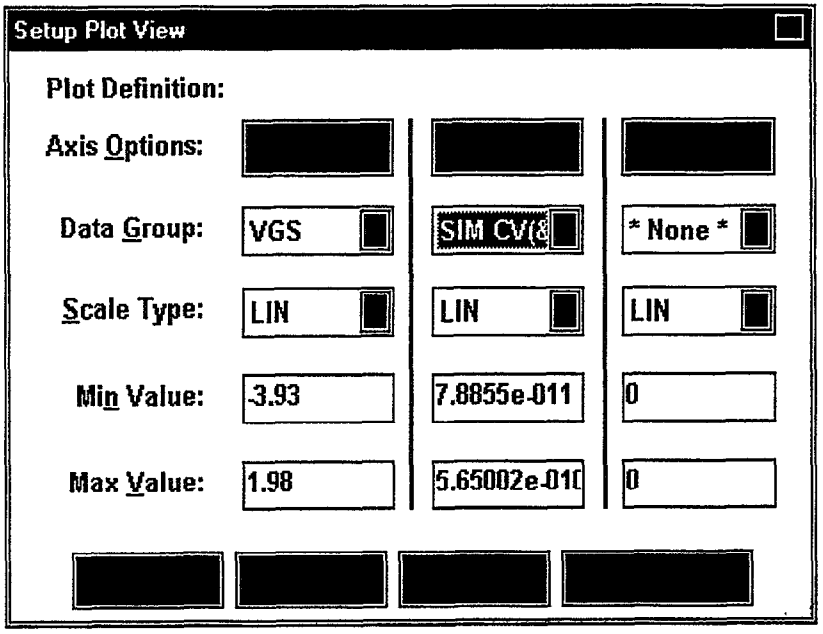


Figure 8 *Setup Plot View Window*

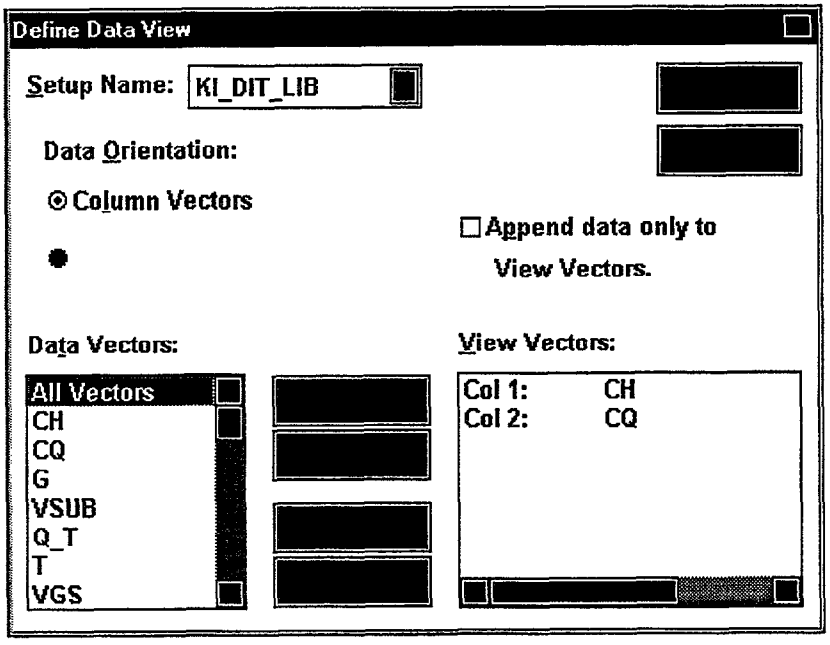


Figure 9 *Build Plot Group Window*

Choose the Right Parameters

Optimal C-V Measurement Parameters

Simultaneous C-V measurement is a complicated matter. Besides system considerations, you should carefully choose the measurement parameters. Refer to the following discussion for considerations when selecting these parameters.

Start, Stop, and Step Voltages

Most C-V data is derived from the steep transition, or depletion region of the C-V curve. For that reason, start and stop voltages should be chosen so that the depletion region makes up about 1/3 to 2/3 of the voltage range. (See Figure 10.)

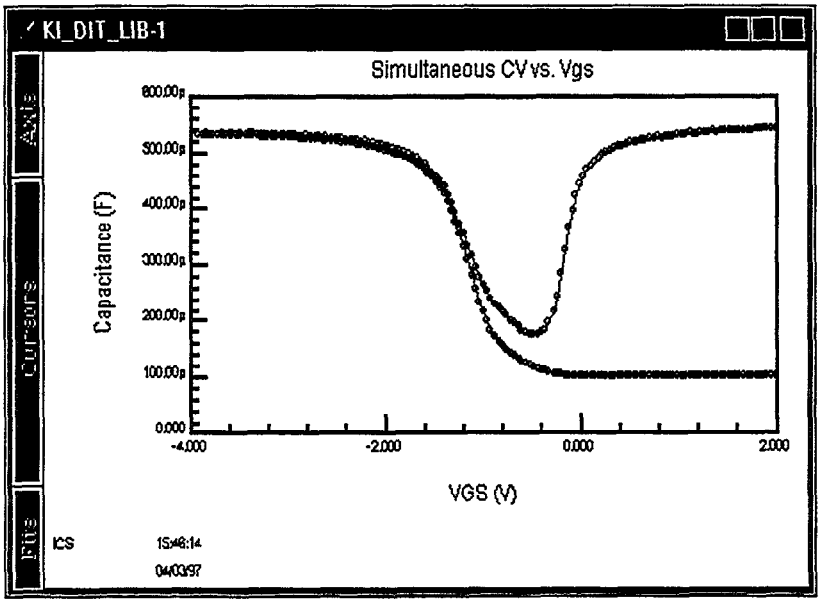


Figure 10 Typical Simultaneous C-V Curve

The upper flat, or accumulation region of the high frequency C-V curve defines the oxide capacitance, C_{OX}. Since most analysis relies on the ratio C/C_{OX}, it is important that you choose a start or stop voltage (depending on the sweep direction) to bias the device into strong accumulation at the start or the end of the sweep.

You should carefully consider the size of the step voltage. Start, stop, and step size determine the total number of data points in the sweep. Some compromise is necessary between having too few data points in one situation, or too many data points in the other.

For example, the complete doping profile is derived from data taken in the depletion region of the curve by using a derivative calculation. As the data point spacing decreases, the vertical point scaling is increasingly caused by noise rather than changes in the desired signal. Consequently, choosing too many points in the sweep will result in increased noise rather than an increased resolution in C-V measurement. It also takes more time to perform a C-V sweep.

Many calculations depend on good measurements in the depletion region, and too few data points in this region will give poor results. A good compromise results from choosing parameters that will yield a capacitance change of approximately ten times the percentage error in the signal.

Sweep Direction

For C-V sweeps, you can sweep either from accumulation to inversion, or from inversion to accumulation. Sweeping from accumulation to inversion will allow you to achieve deep depletion-profiling deeper into the semiconductor than you otherwise would obtain by maintaining equilibrium. When sweeping from inversion to accumulation, you should use a light pulse to achieve equilibrium more rapidly before the sweep begins.

Delay Time

For accurate measurement, delay time must be carefully chosen to ensure that the device remains in equilibrium in the inversion region during a sweep. With too fast a sweep the device will remain in non-equilibrium, affecting Q/t (Figure 11), and also resulting in skewed C-V curves (Figure 12).

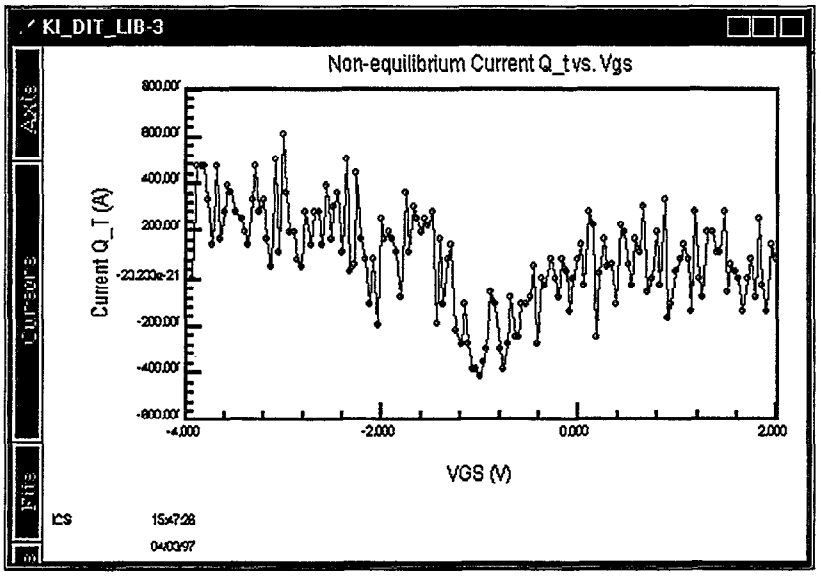


Figure 11 Leakage Current Q/t Through Device

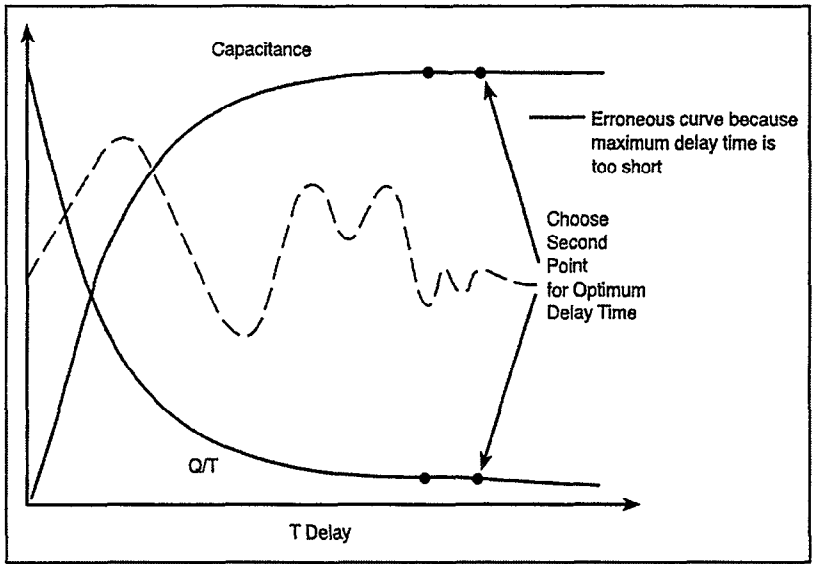


Figure 12 Choosing Optimum Delay Time

Keithley Simultaneous C-V system has a built-in library to help you determine optimal delay time quickly and easily. Refer to the *C-V Libraries and Analysis* chapter for procedures, or use the following procedure to determine optimal delay time.

Determining the Optimal Delay Time

For accurate interface trap density measurement, delay time must be carefully chosen to ensure that the device remains in equilibrium in the inversion region during a sweep.

1. Click on the **Setup Editor** button, then click on the **Source Units** button.

2. Click on the **KI82.OUT** icon to open up the parameter setup window. (See Figure 13.)

3. In the **Mode** section, select the C vs. Delay t measurement.

4. Type in the Start voltage to specify the bias voltage on the DUT during this measurement. Remember that the DUT should be biased in the inversion region for this measurement.

5. Type in the maximum delay times in the Delay (s) box. Note that the total measurement period will be several times longer than the maximum delay time you select.

6. Other parameters should be selected according to your device under test as in the simultaneous C-V measurement example.

7. Click on the **OK** button to exit from this window, then Click on the **Done** button to exit from the **Setup Editor**.

8. Click on the **Meas** button, then click on the **Single** button to start the measurement.

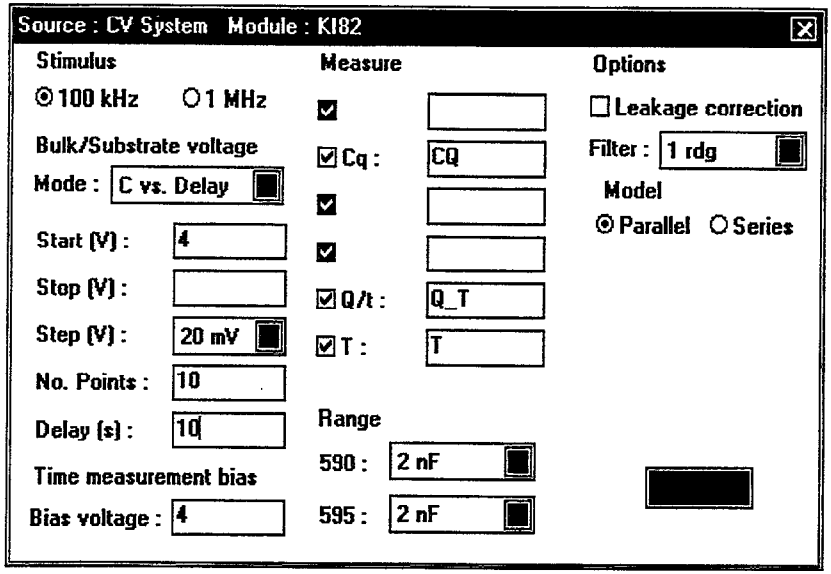


Figure 13 Source Setup Window

Measurement Results

Measurement results will be updated to the data spreadsheet. You may observe them directly. A better way is to plot both Capacitance vs. Delay Time and Q/t vs. Delay Time. Plot both capacitance and Q/t curves. (See Figure 14.) The optimal delay time occurs when both curves flatten out to a slope of zero. For maximum accuracy, choose the second point on the curves after the curve in question has flattened out. For long delay times, the measurement process can become very long with some devices. You may be tempted to speed up the test by using a shorter delay time. However, doing so is not recommended since it is difficult to quantify the amount of accuracy degradation in any given situation.

Determining Delay Time with Leaky Devices

When testing for delay time on devices with relatively large leakage currents, it is recommended that you use the corrected capacitance feature, which is designed to compensate for leakage current. The reason for doing so is illustrated in Figure 15. When large leakage currents are present, the capacitance curve will not flatten out in equilibrium, but will instead either continue to rise (positive Q/t) or begin to decay (negative Q/t).

Using corrected capacitance results in the normal flat capacitance curve in equilibrium due to leakage compensation. Note, however, that the curve taken with corrected capacitance will be distorted in the non-equilibrium region, so data in that region should be considered to be invalid when using corrected capacitance. If it is necessary to use corrected capacitance when determining delay time, it is recommended that you make all measurements on that particular device using corrected capacitance.

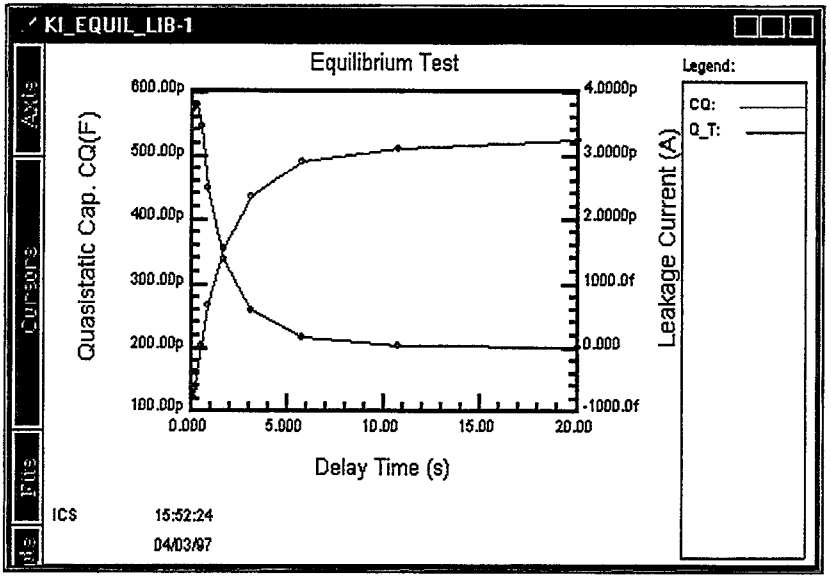


Figure 14 Capacitance and Q/t Curves

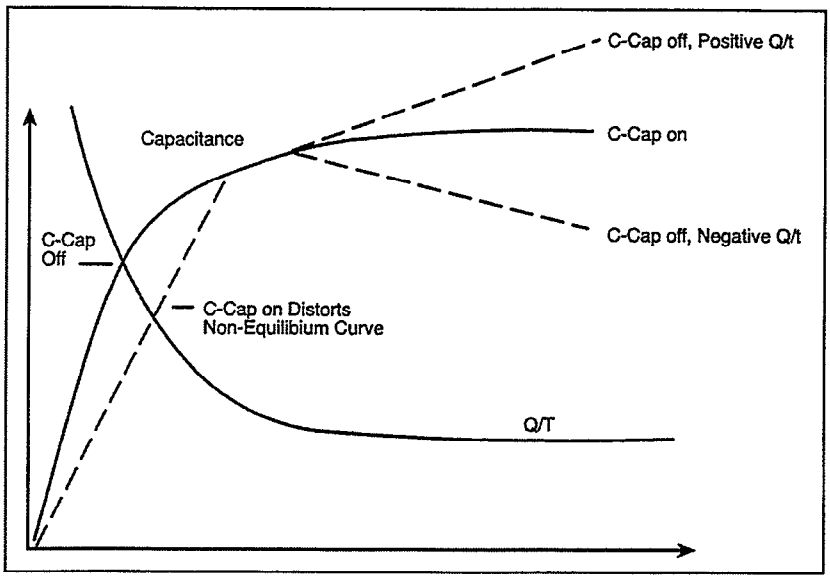


Figure 15 Capacitance and Leakage Current Curves of Leaky Device

Testing Slow Devices

A decaying noise curve, such as the dotted line shown in Figure 12, will result if the maximum delay time is too short for the device being tested. This phenomenon, which is most prevalent with slow devices, occurs because the signal range is too small. To eliminate such erroneous curves, choose a longer maximum delay time. A good starting point for unknown devices is a 30-second maximum delay time.

Additional C-V Measurement Features

Besides making basic simultaneous C-V measurements, there are other features available in the C-V system, including squarewave, single staircase, double staircase, and Capacitance vs. delay time.

Squarewave

The squarewave option lets you select a constant output bias voltage. A squarewave will be output to make the measurement. This feature may be useful for monitoring device change during some time period. Under this option, you may select bias voltage, squarewave step size, and time period.

Staircase

Single Staircase will let you sweep bias voltage in either direction. The Double Staircase option will let you sweep in one direction and then return to the original starting voltage. The sweep step will be the same in both directions. Ideally, if the DUT is in equilibrium during measurement, C-V curves should not exhibit any hysteresis. Hence this option provides you with another means of monitoring the device under test.

Capacitance vs. Delay Time

The Capacitance vs. Delay Time option is very useful to help determine the proper delay time. Detailed procedures are provided in a previous section.

Time Options

There are many different timing options for you to choose. For details, refer to the section on Setup Editor and Measurement in ICS and Keithley C-V driver manuals.

Measurement Considerations

The importance of making careful C-V curve measurements is often underestimated. However, errors in the C-V data will propagate through calculations, resulting in errors in device parameters derived from the curves. These errors can be amplified during calculations by a factor of 10 or more.

With careful attention, the effects of many common error sources can be minimized. In the following paragraphs, we will discuss some common error sources and provide suggested methods for avoiding them.

Potential Error Sources

Theoretically, a capacitance measurement using one of the common techniques would require only that two leads be used to connect the measuring instrument to the device under test (DUT)-the input and output. In practice, however, various parasitic or stray components complicate the measuring circuit.

Stray Capacitances

Regardless of the measurement frequency, stray capacitances present in the circuit are important to consider. Stray capacitances can cause offsets when they are in parallel with the device, can act as a shunt load on the input or output, or can cause coupling between the device and nearby AC signal sources.

When stray capacitance is in parallel with the DUT, it causes a capacitance offset, adding to the capacitance of the device under test (C_{DUT}), as shown in Figure 16. Shunt capacitance, on the other hand, often increases the noise gain of the instrumentation amplifiers, increasing capacitance reading noise (Figure 17). Shunt capacitance also forms a capacitive divider with C_{DUT},

steering current away from the input to ground. This phenomenon results in capacitance gain error, with the C-V curve results shown in Figure 18.

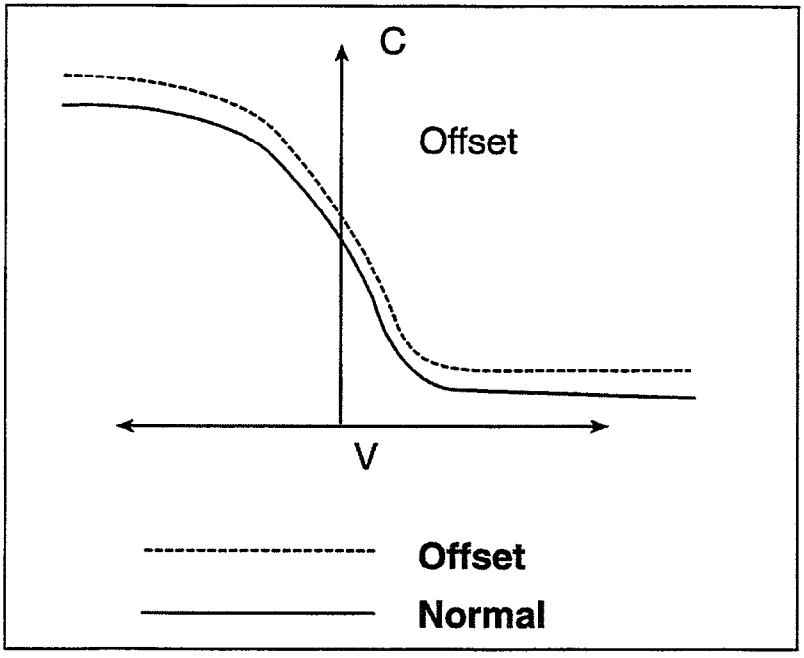


Figure 16 C-V Curve with Capacitance Offset

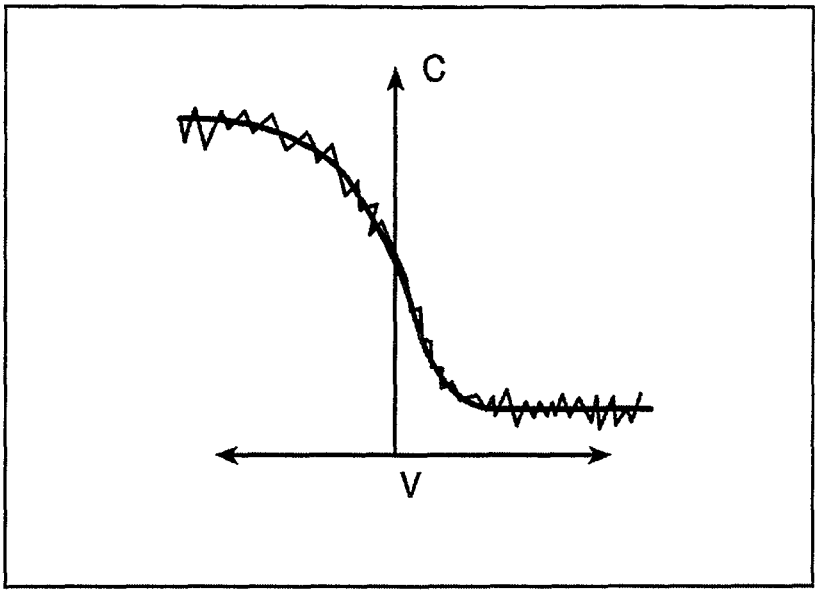


Figure 17 *C-V Curve with Added Noise*

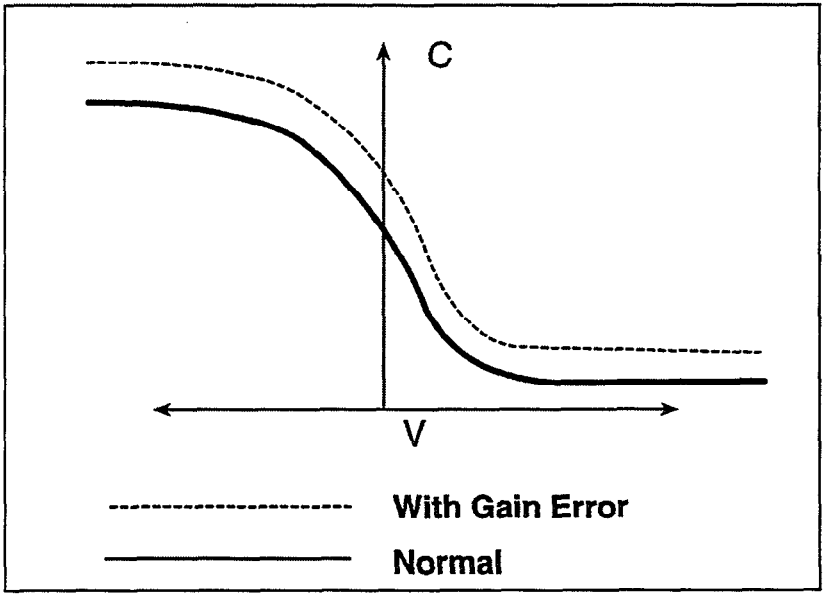


Figure 18 *C-V Curve Resulting from Gain Error*

Stray capacitance may also couple charge current from nearby AC signal sources into the input of the measuring instrument. This noise current adds to the device current and results in noisy or unrepeatable measurements. For quasistatic measurements, power line frequency and electrostatic coupling are particularly troublesome, while digital and RF signals are the primary cause of noise induced in high-frequency measurements.

Leakage Resistances

Under quasistatic measurement conditions, the impedance of C_{DUT} is almost as large as the insulation resistance in the rest of the measurement circuit. Consequently, even leakage resistances of $10^{12}\Omega$ or more can contribute significant errors if not taken into consideration.

Resistance across the DUT will conduct an error current in addition to the device current. Since this resistive current is directly proportional to the applied bias voltage, and the capacitor current is not, the result is a capacitance offset that is proportional to the applied voltage. The end result shows up as a "tilt" in the quasistatic C-V curve, as shown in Figure 19.

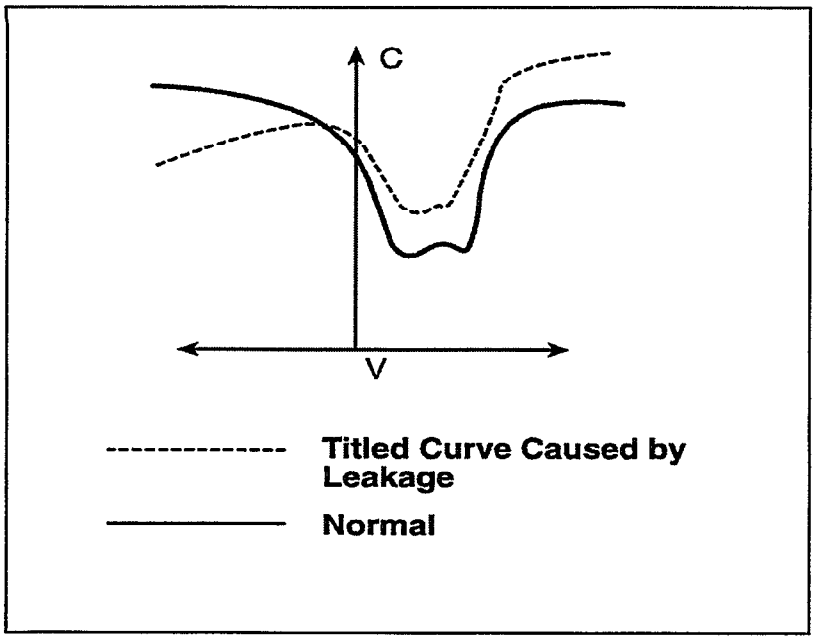


Figure 19 Curve Tilt Caused by Voltage-Dependent Leakage

Stray resistance to nearby fixed voltage sources results in a constant (rather than a bias voltage-dependent) leakage current. Other sources of constant leakage currents include instrument input bias currents, and electrochemical currents caused by device or fixture contamination. Such constant leakage currents cause a voltage-independent capacitance offset.

Keep in mind that insulation resistance is reduced, and leakage current is increased by high humidity as well as by contaminants. In order to minimize these effects, always keep devices and test fixtures in clean, dry conditions.

High-frequency Effects

At measurement frequencies of approximately 100kHz and higher, the impedance of C_{DUT} may be so small that any series impedance in the rest of the circuit may cause errors, Whether such series impedance is caused by inductance (such as from

leads or probes), or from resistance (as with a high-resistivity substrate), this series impedance causes non-linearity in the measured capacitance. The resulting C-V curve is, of course, affected by such non-linearity, as shown in Figure 20.

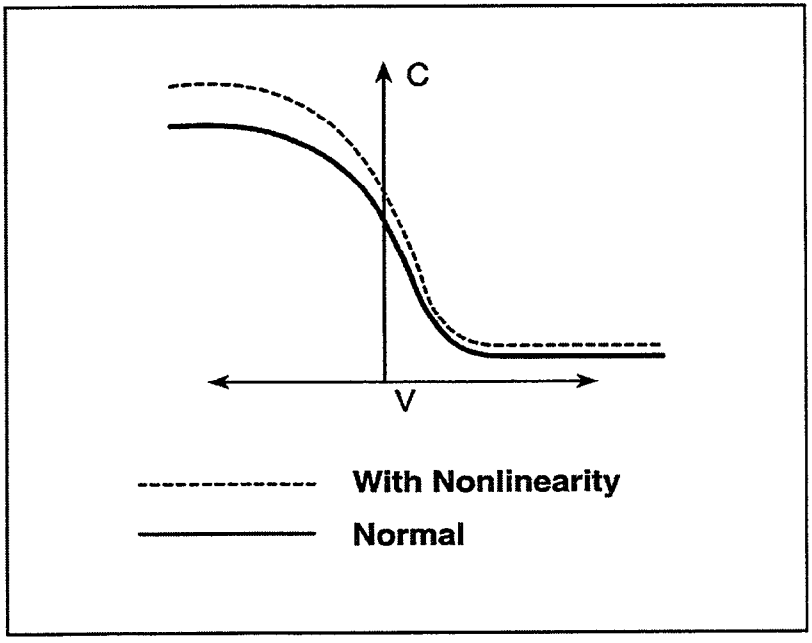


Figure 20 C-V Curve Caused by Nonlinearity

Another high-frequency effect is caused by the AC network formed by the instrumentation, cables, switching circuits, and the test fixtures. Referred to as transmission line error sources, the network essentially transforms the impedance of C_{DUT} when it is referred to the input of the instrument, altering the measured value. Transmission line effects alter the gain and produce non-linearities.

Avoiding Capacitance Errors

Many possible error sources that can affect C-V measurements may seem overwhelming at times, but careful attention to a few key details will reduce errors to an acceptable level. Once most of the error sources have been minimized, any residual errors can be further reduced by using the probe-up suppression and corrected capacitance features.

Key details that require attention include use of proper cabling and effective shielding. These important aspects are discussed below.

Cabling Considerations

Cables must be used to connect the instruments to the device under test. Ideally, these cables should supply the test voltage to the device unaltered in any way. The test voltage is converted into a current or charge in the DUT, and should be carried back to the instruments undisturbed. Along the way, potential error sources must be minimized.

Coaxial cable is usually used in order to eliminate stray capacitance between the measurement leads. The cable shield is connected to a low-impedance point (guard) that follows the meter input. This technique, known as the three-terminal capacitance measurement, is almost universally used in commercial instrumentation. The shield shunts current away from the input to the guard.

Coaxial cables also serve as smooth transmission lines to carry high-frequency signals with minimal attenuation. For this reason, the cable's characteristic impedance should closely match that of the instrument input and output, which is usually 50Ω. Standard RG-58 cable is adequate for frequencies in the range of 1kHz to more than 10MHz. High-quality BNC

connectors with gold-plated center conductors reduce errors from high series contact resistance.

Quasistatic C-V measurements are susceptible to shunt resistance and leakage currents as well as to stray capacitances. Although coaxial cables are still appropriate for these measurements, the cables should be checked to ensure that the insulation resistance is sufficiently high ($>10^{12}\Omega$). Also, when such cables are flexed, the shield rubs against the insulation, generating small currents due to triboelectric effects. These currents can be minimized by using low-noise cable (such as the Model 4801) that is lubricated with graphite to reduce friction and to dissipate generated charges.

Flex-producing vibration should be eliminated at the source whenever possible. If vibration cannot be entirely eliminated, cables should be securely fastened to prevent flexing.

One final point regarding cable precautions is in order: Cables can only degrade the measurement, not improve it. Thus, cable lengths should be minimized where possible, without straining cables or connections.

Device Connections

Care in properly protecting the signal path should not stop at the cable ends where the connection is made to the DUT fixture. In fact, the device connection is an extremely important aspect of the measurement. For the same reasons given for coaxial cables, it is best to continue the coaxial path as close to the DUT as possible by using coaxial probes. Also, it is important to minimize stray capacitance and maximum insulation resistance in the pathway from the end of the coaxial cable to the DUT.

Most devices have one terminal that is well insulated from other conductors, as in the gate of an MOS test dot. The input should be connected to the gate because it is more susceptible to stray signals than is the output. The output can better tolerate being connected to a terminal with high shunt capacitance, noise, or

poor insulation resistance, although these characteristics should still be optimized for best results.

Test Fixture Shielding

At the point where the coaxial cable shielding ends, the sensitive input node is exposed, inviting error sources to interfere. Proper device shielding need not end with the cables or probes, however, if a shielded test fixture is used.

A shielded fixture, sometimes known as a Faraday cage, consists of a metal enclosure that completely surrounds the DUT and leads. In order to be effective, the shield must be electrically connected to the coaxial shield. Typically, bulkhead connectors are mounted to the side of the cage to bring in the signals. Coaxial cables should be continued inside, if possible, or individual input and output leads should be widely spaced in order to maintain input/output isolation.

Correcting Residual Errors

Controlling errors at the source is the best way to optimize C-V measurements, but doing so is not always possible. Remaining residual errors include offset, gain, noise, and voltage-dependent errors. Ways to deal with these error sources are discussed in the following paragraphs.

Offsets

Offset capacitance and conductance caused by the test apparatus can be eliminated by performing a suppression with the probes in the up position. These offsets will then be nulled out when the measurement is made. Whenever the system configuration is changed, the suppression procedure should be repeated. For maximum accuracy, it is recommended that you perform a probes-up suppression or at least verify prior to every measurement.

Gain and Nonlinearity Errors

Gain errors are difficult to quantify. For that reason, gain correction is applied to every measurement. Gain constants are determined by measuring accurate calibration sources during the cable correction process.

Nonlinearity is normally more difficult to correct for than are gain or offset errors. The cable correction utility, however, provides nonlinearity compensation for high-frequency measurements, even for non-ideal configurations such as switching matrices.

Voltage-dependent Offset

Voltage-dependent offset (curve tilt) is the most difficult to correct error associated with quasistatic C-V measurements. It can be eliminated by using the corrected capacitance function of the software. In this technique, the current flowing in the device is measured as the capacitance value is measured. The current is known as Q/t because its value is derived from the slope of the charge integrator waveform. Q/t is used to correct capacitance readings for offsets caused by shunt resistance and leakage currents.

Care must be taken when using the corrected capacitance feature, however. When the device is in non-equilibrium, device current adds to any leakage current, with the result that the curve is distorted in the non-equilibrium region. The solution is to keep the device in equilibrium throughout the sweep by carefully choosing the delay time.

Curve Misalignment

At times, quasistatic and high frequency curves may be slightly misaligned due to gain errors or external factors. In such cases, curve gain and offset factors can be applied to the curves to properly align them..

Noise

Residual noise on the C-V curve can be minimized by using filtering when taking your data. However, the filter will reduce the sharpness of the curvature in the transition region of the quasistatic curve depending on the number of data points in the region. This change in the curve can cause C_Q to dip below C_H resulting in erroneous D_{IT} calculations. If this situation occurs, turn off the filter or add more data points.

Interpreting C-V Curves

Even when all the precautions outlined here are followed, there are still some possible obstacles to successfully using C-V curves to analyze semiconductor devices.

Semiconductor capacitances are far from ideal, so care must be taken to understand how the device operates. Also, the curves must be generated under well-controlled test conditions that ensure repeatable, analyzable results.

Maintaining Equilibrium

The condition of the device when all internal capacitances are fully charged is referred to as equilibrium. Most quasistatic and high-frequency C-V curve analysis is based on the simplified assumption that the device is measured in equilibrium. Internal RC time constants limit the rate at which the device bias may be swept while maintaining equilibrium. They also determine the hold time required for device settling after setting the bias voltage to a new value before measuring C_{DUT}.

The two main measurement parameters that affect equilibrium, then, are the bias sweep rate and the hold time. When these parameters are set properly, the normal C-V curves shown in Figure 21 result. Once the proper sweep rate and hold time have been determined, it is important that all curves compared with one another be measured under the same test conditions; otherwise, it may be the parameters, not the devices themselves, that cause the compared curves to differ.

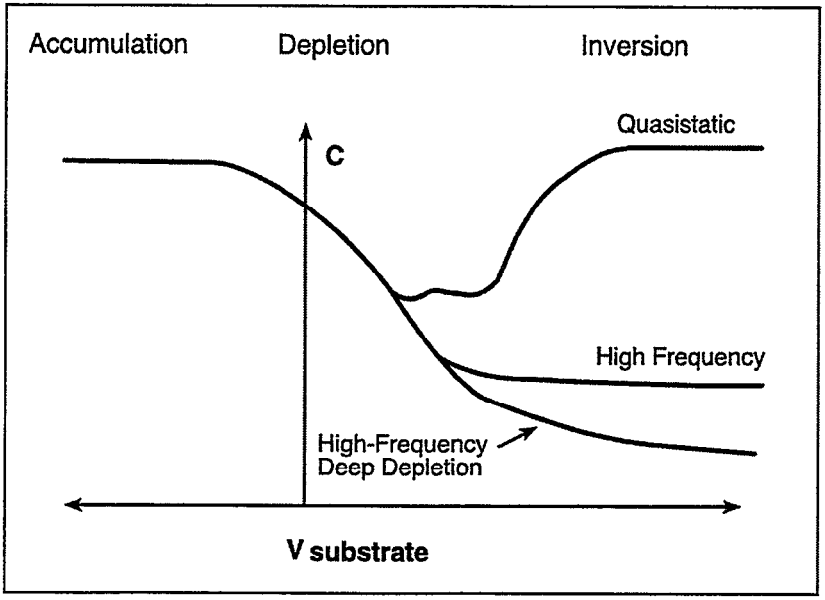


Figure 21 Normal C-V Curves

Analyzing Curves for Equilibrium

There are three primary indicators that can be used to determine whether a device has remained in equilibrium during testing. First, as long as a device is in equilibrium, C_{DUT} is settled at all points in the sweep. As a result, it makes no difference whether the sweep goes from accumulation to inversion, or from inversion to accumulation, nor does it matter how rapidly the sweep is performed. Therefore, curves made in both directions will be the same, exhibiting no hysteresis, and any curve made at a slower rate will be the same. Figure 22 shows the type of hysteresis that will occur if the sweep rate is too fast, and the device does not remain in equilibrium.

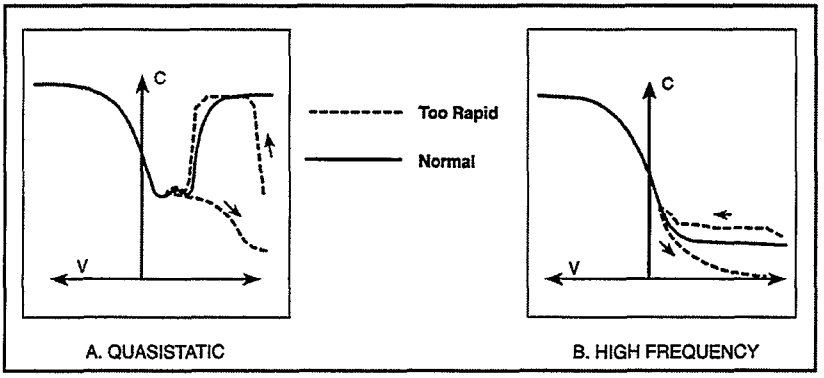


Figure 22 *Curve Hysteresis with Sweep too Rapid*

The second equilibrium factor requires that the DC current through the device be essentially zero at each measurement point after device settling. This test can be performed by monitoring Q/t.

Thirdly, the curves should exhibit the smooth equilibrium shape. Deviations from the ideal smooth shape indicate a non-equilibrium condition, as in the examples resulting from too short a hold time shown in Figure 23. Note that at least two of

these indicators should be used together, if possible, because any one of the three alone can be misleading at times.

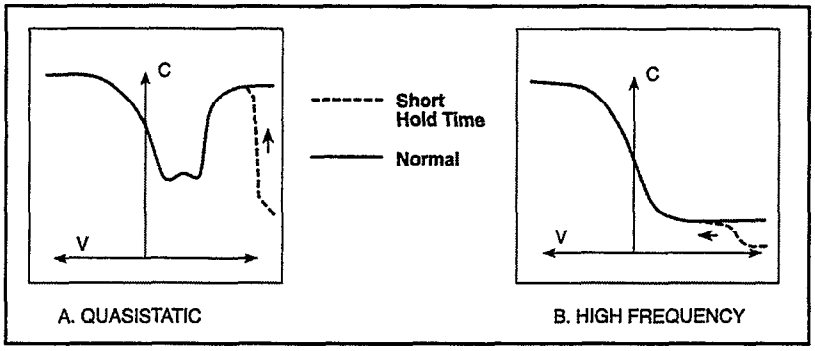


Figure 23 Curve Distortion with Hold Time too Short

One final quick test to confirm equilibrium is to observe C_Q during a hold time at the end of the C-V sweep from accumulation to inversion. During this final hold time, the capacitance should remain constant. If a curve has been swept too quickly, the capacitance will rise slightly during the final hold time.

Initial Equilibrium

Biasing the device to the starting voltage in the inversion region at the beginning of a C-V measurement creates a non-equilibrium condition that must be allowed to subside before the C-V sweep begins. This recovery to equilibrium can take seconds, minutes, or even tens of minutes to achieve. For that reason, it is generally advantageous to begin the sweep in the accumulation region of the curve whenever possible.

Still, it is often necessary to begin the sweep in the inversion region to check for curve hysteresis. In this case, a light pulse, shone on the device, can be used to quickly generate the minority carriers required by the forming inversion layer, thus speeding up equilibrium and shortening the hold time.

The best way to ensure equilibrium is initially achieved is to monitor the DC current in the device and wait for it to decay to the DC leakage level of the system. A second indication that equilibrium is reached is that the capacitance level at the initial bias voltage decays to its equilibrium level.

Dynamic Range Considerations

The dynamic range of a suppressed quasistatic of high-frequency measurement will be reduced by the amount suppressed. For example, if, on the 200pF range, you were to suppress a value of 10pF, the dynamic range would be reduced by that amount. Under these conditions, the maximum value the instrument could measure without overflowing would be 190pF.

A similar situation exists when using cable correction with the Model 590. For example, the maximum measurable value on the 2nF range may be reduced to 1.8nF when using cable correction. The degree of reduction will depend on the amount of correction necessary for the particular test setup.

The dynamic range of quasistatic capacitance measurements is reduced with high Q/t. The maximum Q/t value for a given capacitance value depends on both the delay time and the step voltage. See the Model 595 Instruction Manual Specifications for details.

Series and Parallel Model Equivalent Circuits

A complex impedance can be represented by a simple series or parallel equivalent circuit made up of a single resistive element and a single reactive element, as shown in Figure 24. In the parallel form of (a), the resistive element is represented as the conductance, G, while the reactance is represented by the susceptance, B. The two together mathematically combine to give the admittance, Y, which is simply the reciprocal of the circuit impedance.

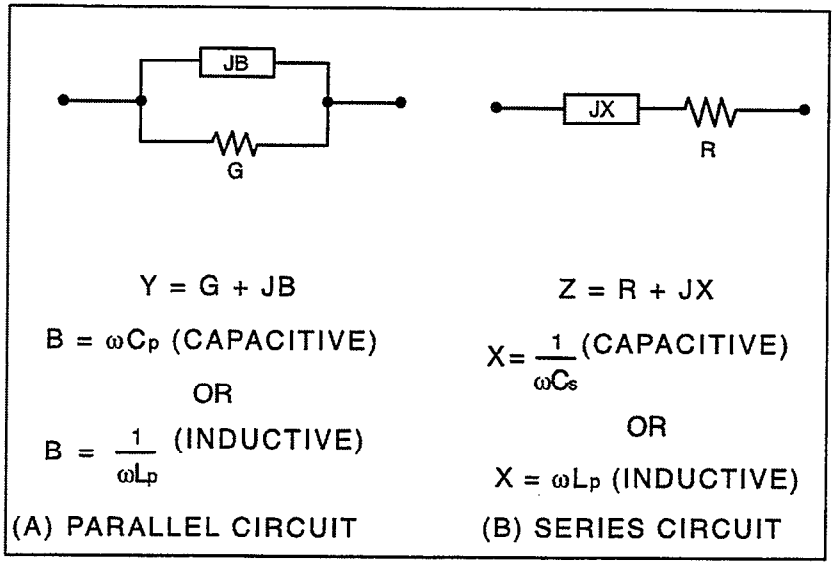


Figure 24 Series and Parallel Circuits

In a similar manner, the resistance and reactance of the series form of (b) are represented by R and X, respectively. The impedance of the series circuit is Z.

The net impedances of the equivalent series and parallel circuits at a given frequency are equal. However, the individual components are not. We can demonstrate this relationship mathematically as follows:

$$R + jX = \frac{1}{G + jB}$$

To eliminate the imaginary form in the denominator of the right-hand term, we can multiply both the denominator and numerator by the conjugate of the denominator as follows:

$$R + jX = \frac{1}{G + jB} \times \frac{G - jB}{G - jB}$$

Performing the multiplication and combining terms, we have:

$$R + jX = \frac{G - jB}{G^2 + B^2}$$

If we assume the reactance is capacitive, we can use $-1/\omega C_S$ for the reactance and ωC_P for the susceptance (C_S is the equivalent series capacitance, and C_P is the equivalent parallel capacitance). The above equation then becomes:

$$\frac{R - jX}{\omega C_S} = \frac{G - j\omega C_P}{G^2 + \omega^2 C_P^2}$$

In a lossless circuit (R and G both 0), C_P and C_S would be equal. A practical circuit, however, does have loss be cause of the finite values of R or G. Thus, C_S and C_P are not equal – the greater the circuit loss, the larger the disparity between these two values.

Series and parallel capacitance values can be converted to their equivalent forms by taking into account a dissipation factor, D, which is simply the reciprocal of the Q of the circuit. For a parallel circuit, the dissipation factor is:

$$D = \frac{1}{Q} = \frac{G}{\omega C_P}$$

For the series circuit, the dissipation factor is defined as:

$$D = \frac{1}{Q} = \omega C_S R$$

By using the dissipation factor along with the formulas summarized in Table 1, you can convert from one form to another. Note that C_S and C_P are virtually identical for very small values of D. For example, if D is 0.01 C_S and C_P are within 0.01% of one another.

Table 1 Converting series-parallel equivalent circuits

Model	Dissipation factor	Capacitance	Resistance or conductance
Parallel C_P, G	$D = \frac{1}{Q} = \frac{G}{\omega C_P}$	$C_S = (1 + D^2)C_P$	$R = \frac{D^2}{(1 + D^2)G}$
Series C_S, R	$D = \frac{1}{Q} = \omega C_S R$	$C_P = \frac{C_S}{1 + D^2}$	$G = \frac{D^2}{(1 + D^2)R}$

Example

Assume that we make a 100kHz measurement on a parallel equivalent circuit and obtain values for C_P and G of 160pF and 30μS respectively. From these values, we can calculate the dissipation factor, D, as follows:

$$D = \frac{30 \times 10^{-6}}{2\pi(100 \times 10^{3})(160 \times 10^{-12})}$$

$$D = 0.3$$

The equivalent series capacitance is then calculated as follows:

$$C_S = (1 + 0.09)160pF$$

$$C_S = 174.4pF$$

Device Considerations

Series Resistance

Devices with high series resistance can cause measurement and analysis errors unless steps are taken to compensate for this error term. The high dissipation factor caused by series resistance can cause errors in C_{OX} measurement, resulting in errors in analysis functions (such as doping concentration) that use C_{OX} for calculations.

The software uses a three-element model to compensate for series resistance. The series resistance, R_{SERIES} is an analysis constant that can be determined using the procedure covered previously.

The software determines the displayed value of R_{SERIES} by converting parallel model data from the Model 590 into series model data. The resistance value corresponding to the maximum high-frequency capacitance in accumulation is defined as R_{SERIES}.

Device Structure

The standard analysis assumes a conventional MOS structure made up of silicon substrate, silicon dioxide insulator, and aluminum gate material. You can change the program for use with other types of materials by modifying the material constants using the Transform editor. For compound materials, a weighted average of pertinent material constants is often used. Typical compound materials include silicon nitride and silicon dioxide in a two- or three-layer sandwich.

Device Integrity

In order for analysis to be valid, device integrity should be checked before measurement. Excessive leakage current through the oxide can bleed off the inversion layer, causing the device to remain in non-equilibrium indefinitely. In this situation, the inversion layer would never form completely, and C_{MIN} measurements would be inaccurate.

Device integrity can be verified by monitoring Q/t levels. If Q/t levels are excessive, device integrity is suspect.

Test Equipment Considerations

Light Leaks

High-quality MOS capacitors, which are the subject of C-V analysis, are excellent light detectors. Consequently, care should be taken to ensure that no light leaks into the test fixture or probe station. Typical areas to check include door edges and hinges, tubing entry points, and connectors or connector panels.

Thermal Errors

Accurate temperature control is important for accurate C-V data. For example, the intrinsic carrier concentration, doubles for every 8°C increase in ambient temperature. In order to minimize the effects of thermal errors, keep the device at a constant temperature during measurement, and repeated measurements should all be made at the same temperature.

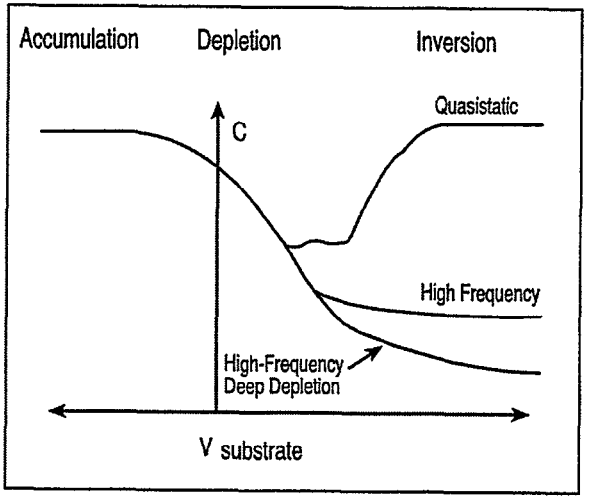
If you change the measurement temperature, change the material constants for correct values for temperature and intrinsic concentration using the Transform editor.

User's Guide

Model 82-WIN Simultaneous C-V Libraries and Analysis

Keithley Instruments, Inc.

Release Date: April 1997



Contents

C-V Libraries and Analysis

Introduction

The Keithley Simultaneous C-V System Model 82-WIN is equipped with many measurement and analysis libraries that can help you extract a large amount of information from your simultaneous C-V measurement data quickly and easily. This chapter covers using these libraries to suit your measurement and analysis needs. It is organized as follows:

Using Keithley Simultaneous C-V Libraries: Outlines the procedures for making measurements and analyzing data effectively.

Analysis Methods: Discusses methods of extracting parameters from simultaneous C-V curves. It also includes in-depth discussion of several methods to determine mobile ion charge concentration.

Constants, Symbols, and Equations Used for Analysis: Lists the material constants used in calculations and shows how to modify the constants. Raw and calculated data symbols used in the libraries are listed. Equations are also listed.

References and Bibliography of C-V Measurements: Summarizes references for C-V measurement and analysis, along with additional texts and papers for suggested reading.

Using Keithley Simultaneous C-V Libraries

Determining Interface Trap Density

Interface trap charge is important in determining device integrity. In fabrication environments, trap density must be carefully controlled. Interface trapped charge can be of several types: (1) structural, oxidation-induced defects; (2) metal impurities; and (3) other defects caused by radiation or bond-breaking processes. The interface trapped charge is located at the Si-SiO_2 interface. It is in electrical proximity to the underlying silicon, which can be either charged or discharged.

The Keithley Interface trap density (D_{IT}) library can perform interface trapped charge density analysis. It has a built-in correction algorithm to eliminate the problems associated with leakage current. Many parameters can also be extracted from this measurement, including doping profile, flatband voltage and capacitance, threshold voltage, work functions, and oxide charge.

Steps for Using Interface Trap Density Library

Step 1: Load the Keithley Interface Trap Density Library into ICS

Use the **Import** command under the **File** menu to import the Keithley D_{IT} library named KI_DIT.DAT. Your screen should look like the one shown in Figure 1.

Step 2: Modify Measurement Parameters

1. Click on the **Setup Editor** button.
2. Click on the **KI_82.OUT** icon. You should now be in the parameter setup window.
3. Type in the appropriate measurement parameters.
4. Close all windows to return to the main window.

Step 3: Modify Analysis Library Constants

1. Click on the **Transform Editor** button.
2. Click on the **Edit Constants** button.
3. Select and type in the constants you wish to change.
4. Return to the main window by clicking on the **OK** and **DONE** buttons in that order.

Step 4: Make the Measurement

1. Click on the **Zero Cancel** button to do a probe-up suppress.
2. Click on the **Single** button on the Measurement menu to take the measurement.

3. You may view the results directly on the screen shortly after data is taken,. Several plots are available on screen, and you may expand them to examine details, or you may create your own plot. Available plots are: capacitance curves, leakage current curve, band bending, and doping profile. All measured and calculated data are displayed in the data spreadsheet window.

Typical Measurement Results

A typical simultaneous C-V measurement is shown in Figure 1. Figure 2 shows the device leakage current, which can be a valuable tool to monitor system performance and device integrity. Interface trap density for this particular device is shown in Figure 3, and band bending vs. gate voltage and doping profile vs. gate voltage are also plotted.

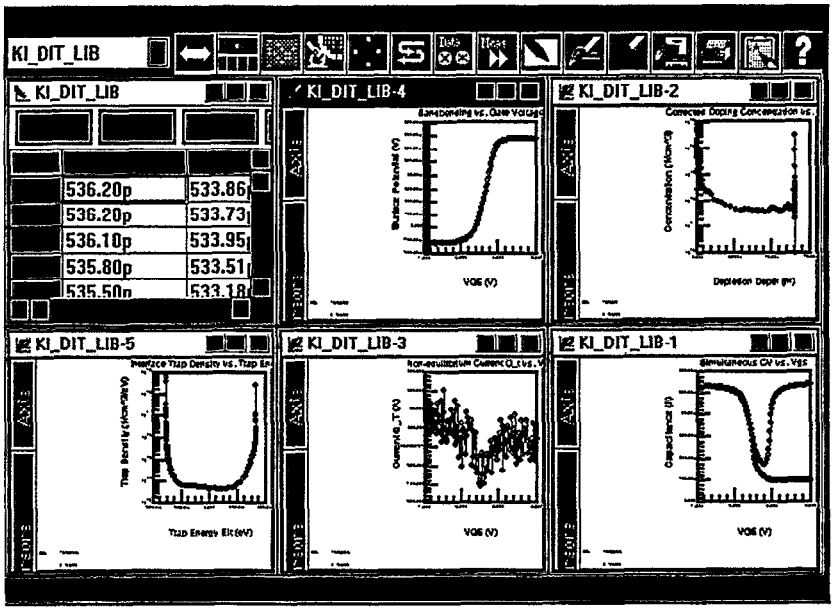


Figure 1 Interface Trap Density Library Main Windows

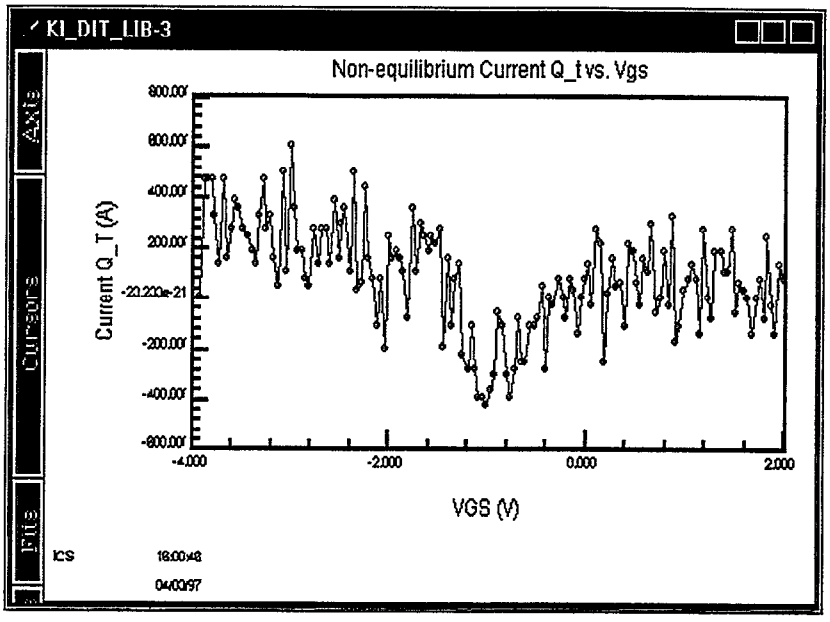


Figure 2 Device Leakage Current Plot

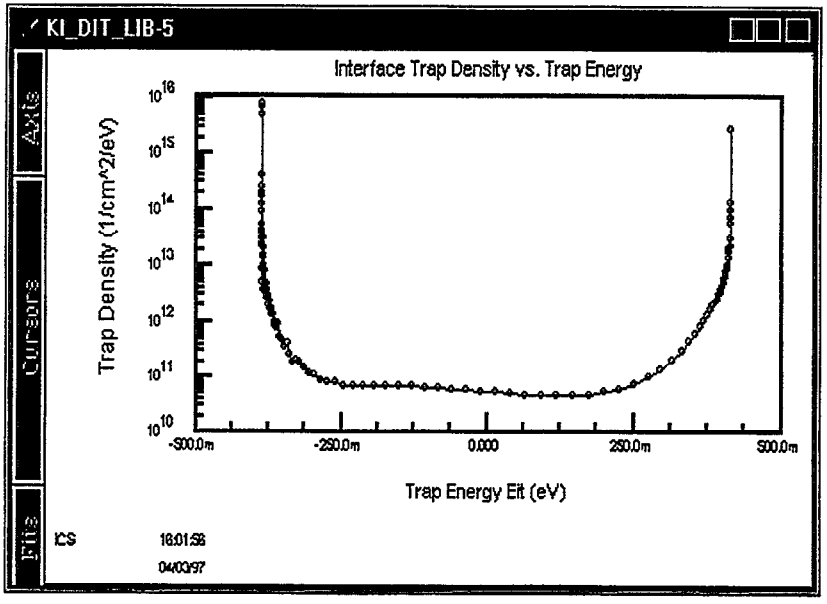


Figure 3 Interface Trap Density Plot

Mobile Ion Charge Monitoring with Simultaneous Triangular Voltage Sweep (STVS) Technique

STVS is a new technique developed by Keithley to monitor mobile ion charge in MOS structures. Compared with other mobile ion monitoring techniques, such as the BTS and flatband shift methods, it offers faster and more accurate measurement. STVS measures ionic current instead of voltage shift. It has the ability to identify species, and it eliminates the need for temperature cycling of the Device Under Test (DUT). The STVS method has proven to be effective in monitoring mobile ions in dielectrics at levels down to $10^9 cm^{-3}$.

The STVS library can perform the corresponding mobile ion charge analysis. It has a built-in correction algorithm to eliminate the problems associated with leakage current. Many parameters, including mobile ion charge concentration, can be extracted from this measurement.

Steps for Using Mobile Ion Charge Library

Step 1: Heat the DUT to the Desired Temperature

Heat the DUT to the desired temperature before testing. 250-300°C should be sufficient for sodium ions in most cases.

Step 2: Load the Keithley STVS Library

Using the **Import** command under the **File** menu, import the Keithley STVS library named KI_M_ION.DAT. Your screen should look like the one shown in Figure 4.

Step 3: Modify Measurement Parameters

1. Click on the **Setup Editor** button, and then click on the **KI_82.OUT** icon. You should now be in the parameter setup window.

2. Type in the appropriate measurement parameters, then close all the windows to return to the main window.

Step 4: Modify Analysis Library Constants

1. Click on the **Transform Editor** button.

2. Click on the **Edit Constants** button.

3. Select and type in the constants you wish to change.

4. Return to the main window by clicking on the **OK** and **DONE** buttons in that order.

Step 5: Make the Measurement

1. Click on the **Zero Cancel** button to do a probe-up suppress.

2. Click on the **Single** button on the Measurement menu to take the measurement.

3. Results will be displayed shortly after data is taken. Capacitance curves and the leakage current curve are displayed, and all measured and calculated data are displayed in the data spreadsheet window.

Typical Measurement Results

Figure 4 shows a mobile ion plot. A typical Simultaneous C-V measurement at elevated temperature is shown in Figure 5. Note that the curve peak is caused by mobile ion charge in the dielectric. You may also wish to check leakage current for measurement integrity. For this particular device, the mobile ion concentration can be obtained from the plot.

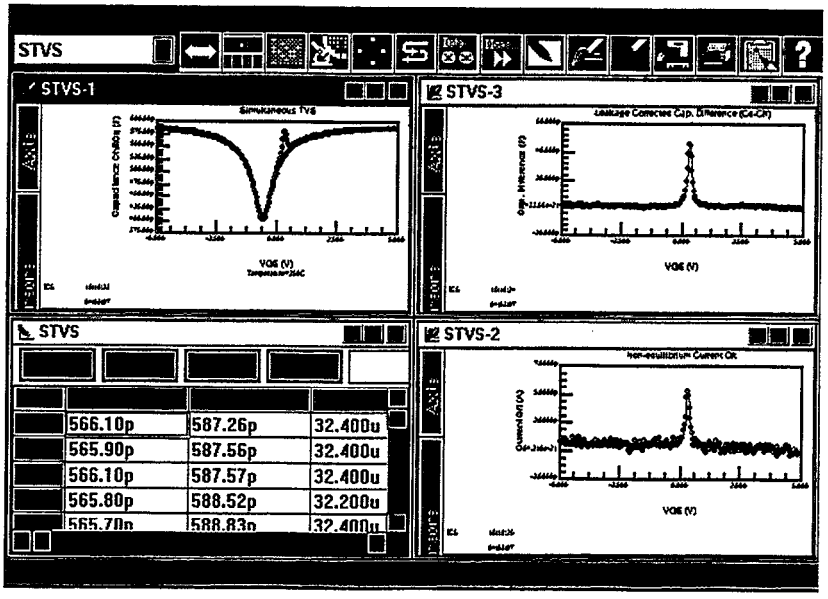


Figure 4 Mobile Ion Charge Plot

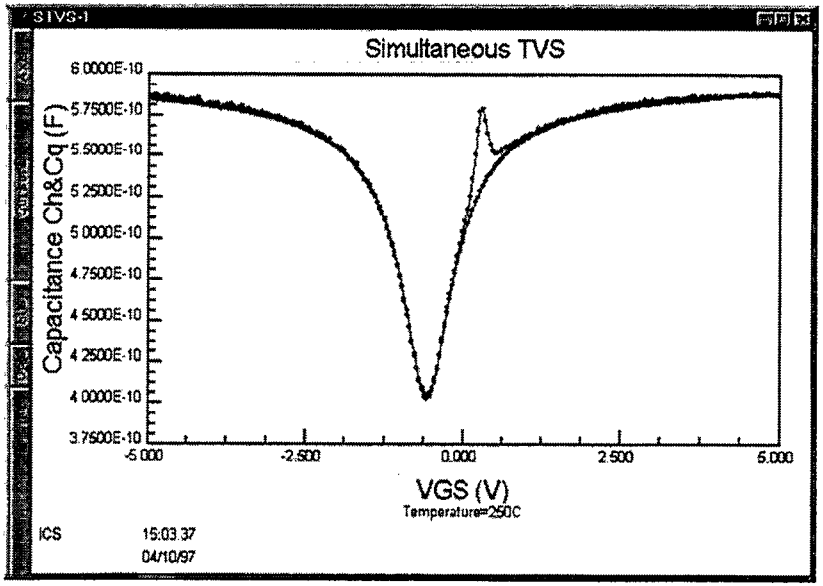


Figure 5 Simultaneous C-V Curve at Elevated Temperature

Determining Doping Profile with High-frequency C-V

Doping profile is one of the important parameters for many semiconductor devices. It is normally derived from C-V measurements, although it is also related to resistivity. It can be extracted from a high-frequency C-V curve using the Keithley Model 590 High Frequency Capacitance measurement package.

Steps for Using Doping Profile Library

Step 1: Load the Keithley High-frequency C-V Library

Using the **Import** command under the **File** menu, import the Keithley high-frequency C-V library named KI_DOPE.DAT. Your screen should look like the one shown in Figure 6.

Step 2: Modify Measurement Parameters

1. Click on the **Setup Editor** button.
2. Click on the **KI_82.OUT** icon. You should now be in the parameter setup window.
3. Type in the appropriate measurement parameters.
4. Close all windows to return to the main window.

Step 3: Modify Analysis Library Constants

1. Click on the **Transform Editor** button.
2. Click on the **Edit Constants** button.
3. Select and type in the constants you wish to change.
4. Return to the main window by clicking on the **OK** and **DONE** buttons in that order.

Step 4: Make the Measurement

1. Click on the **Zero Cancel** button to do a probe-up suppress.
2. Click on the **Single** button on the Measurement menu to take the measurement.
3. You may view the results shortly after data is taken. Several plots are available on the screen, and you may expand them to examine details. Available plots are: capacitance curves, leakage current curve, band bending, and doping profile. All data, including measured and calculated data, are displayed in the data spreadsheet window.

Typical Measurement Results

A typical doping profile plot is shown in Figure 6. Figure 7 shows doping profile obtained from high-frequency C-V measurement. You may also wish to check leakage current to monitor system performance and device integrity. With this

library, device doping profile, depletion vs. gate voltage and $1/C_H^2$ vs. gate voltage are also shown.

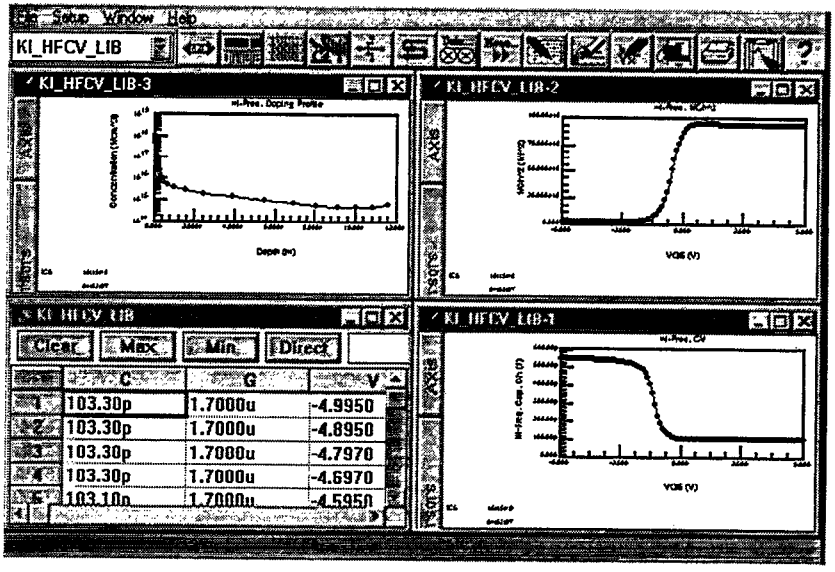


Figure 6 *High-frequency Doping Profile Plot*

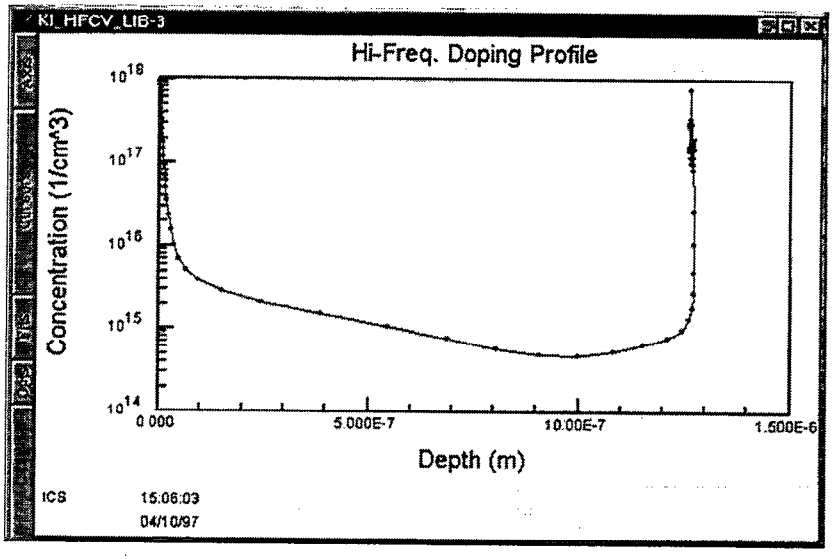


Figure 7 *Doping Profile Derived from High-frequency C-V Measurement*

Determining Equilibrium State

The condition of the device when all internal capacitance is fully charged is referred to as the equilibrium state. Most simultaneous C-V analysis is based on the assumption that the device is measured in equilibrium. Thus, while making a C-V measurement, it is very important that the device remain in equilibrium throughout the sweep. Internal RC time constants limit the rate at which the device bias may be swept. They also determines the hold time required for device settling after setting the bias to a new value before measuring capacitance.

The Keithley Equilibrium library helps you to determine optimum delay time easily. At equilibrium, the capacitance should reach a stable value, and device leakage current should be very close to zero.

Steps for Using Equilibrium State Test Library

Step 1: Load the Keithley Equilibrium Library

Using the **Import** command under the **File** menu, import the Keithley Equilibrium library named KI_EQUIL.DAT. Your screen should look like the one shown in Figure 8.

Step 2: Modify Measurement Parameters

1. Click on the **Setup Editor** button.
2. Click on the **KI_82.OUT** icon. You should now be in the parameter setup window.
3. Type in the appropriate measurement parameters.
4. Close all windows to return to the main window.

Step 3: Make the measurement

1. Click on the **Zero Cancel** button to do a probe-up suppress.
2. Click on the **Single** button on the Measurement menu to take the measurement.
3. You may view the results shortly after data is taken, and you may expand the plot to examine details. All data, include measured and calculated data, are displayed in the data spreadsheet window.

Typical Measurement Results

A typical equilibrium measurement is shown in Figure 8. Also shown is the device leakage current during measurement, which can be a valuable tool to monitor system performance and device integrity.

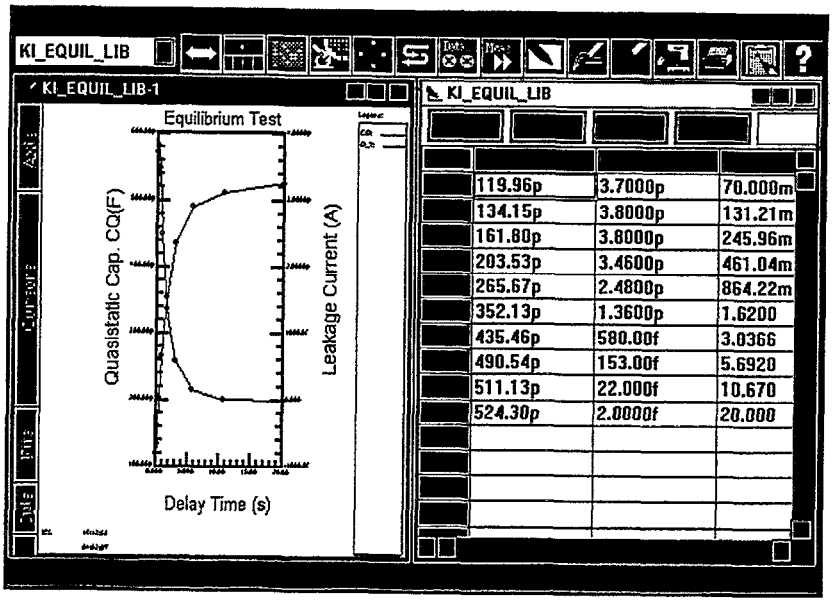


Figure 8 Equilibrium State Test Plot

Analysis Methods

This section discusses the theory and techniques used in the various Keithley Simultaneous C-V libraries. For more detailed discussions, refer to the references at the end of the chapter. A text file named EQUATION.TXT lists all the equations used in Keithley libraries is provided, and another file named CONSTANT.TXT lists the constants used in Keithley libraries.

Basic Simultaneous C-V Curves

Figure 9 and Figure 10 show fundamental C-V curves for p-type and n-type materials respectively. Both high-frequency and quasistatic curves are shown in these figures. Note that the high-frequency curves are highly asymmetrical, while the quasistatic curves are almost symmetrical. Accumulation, depletion, and inversion regions are also shown on the curves. The gate-biasing polarity and high-frequency curve shape can be used to determine device type, as discussed below.

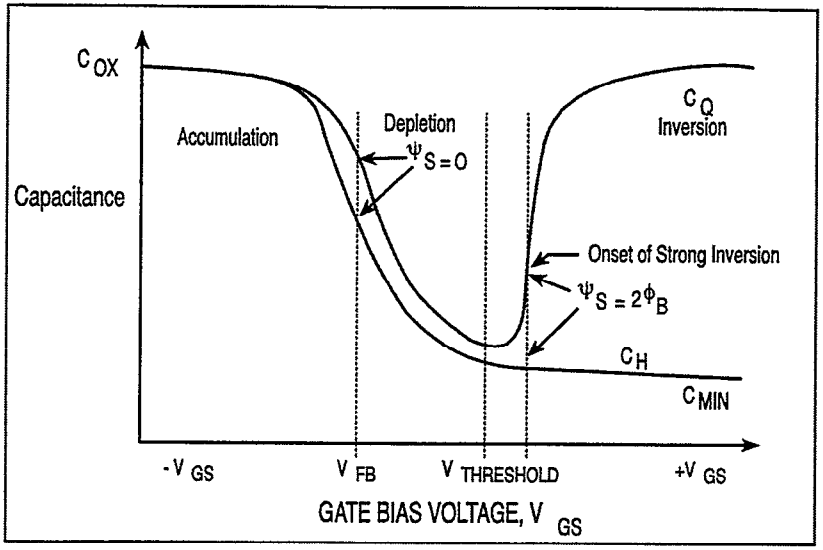


Figure 9 C-V Characteristics of p-type Material

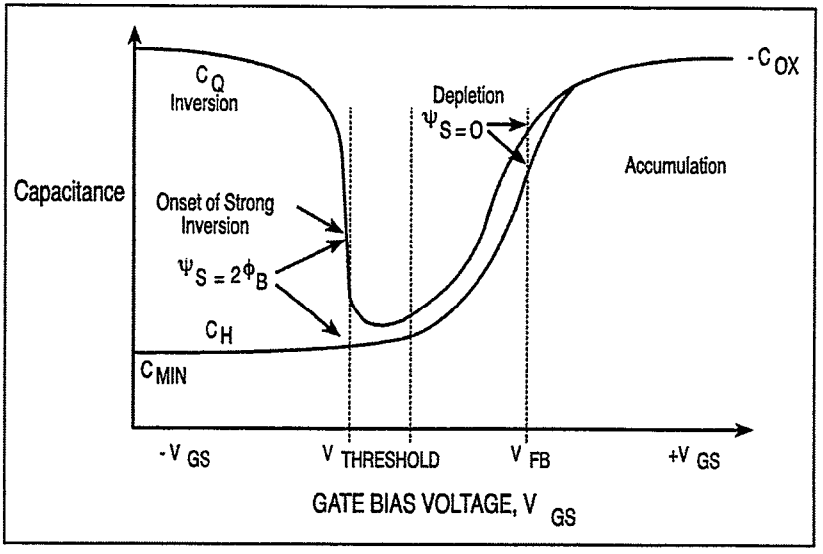


Figure 10 C-V Characteristics of n-type Material

Basic Device Parameters

Determining Device Type

The semiconductor conductivity type (p or n dopant ions) can be determined from the relative shape of the C-V curves. (See Figure 9 and Figure 10.) The high-frequency curve gives a better indication than the quasistatic curve because of its highly asymmetrical nature. Note that the C-V curve moves from the accumulation to the inversion region as gate voltage, V_{GS}, becomes more positive for p-type materials, but the curve moves from accumulation to inversion as V_{GS} becomes more negative with n-type materials (Nicollian and Brews 372-374).

1. If C_H is greater when V_{GS} is negative than when V_{GS} is positive, the substrate material is p-type.

2. If, on the other hand, C_H is greater with positive V_{GS} than with negative V_{GS}, the substrate is n-type.

3. The end of the curve where C_H is greater is the accumulation region, while the opposite end of the curve is the inversion region. The transitional area between these two is the depletion region. These areas are marked on Figure 7 and Figure 8.

Oxide Capacitance, Thickness, and Gate Area

The oxide capacitance, C_{OX}, is the high-frequency capacitance with the device biased in strong accumulation. Oxide thickness is calculated from C_{OX} and gate area as follows:

$$t_{OX} = \frac{A \in_{OX}}{\left(1 \times 10^{-19}\right) C_{OX}} \qquad (1)$$

Where:

t_{OX} = oxide thickness (nm)

A = gate area (cm^2)

$\in_{OX}$ = permittivity of oxide material (F/cm)

C_{OX} = oxide capacitance (pF)

The above equation can be easily rearranged to calculate gate area if the oxide thickness is known. Note that $\in_{OX}$ and other constants are initialized for use with silicon substrate, silicon dioxide insulator, and aluminum gate material but may be changed for other materials. (See *Modifying Constants* near the end of this chapter.)

Series Resistance

The series resistance, R_{SERIES} is an error term that can cause measurement and analysis errors unless this series resistance error factor is taken into account. Without series compensation, capacitance can be lower than normal, and C-V curves can be distorted. The software compensates for series resistance using the simplified three-element model shown in Figure 11. In this model, C_{OX} is, of course, the oxide capacitance while C_A is the capacitance of the accumulation layer. The series resistance is represented by R_{SERIES}.

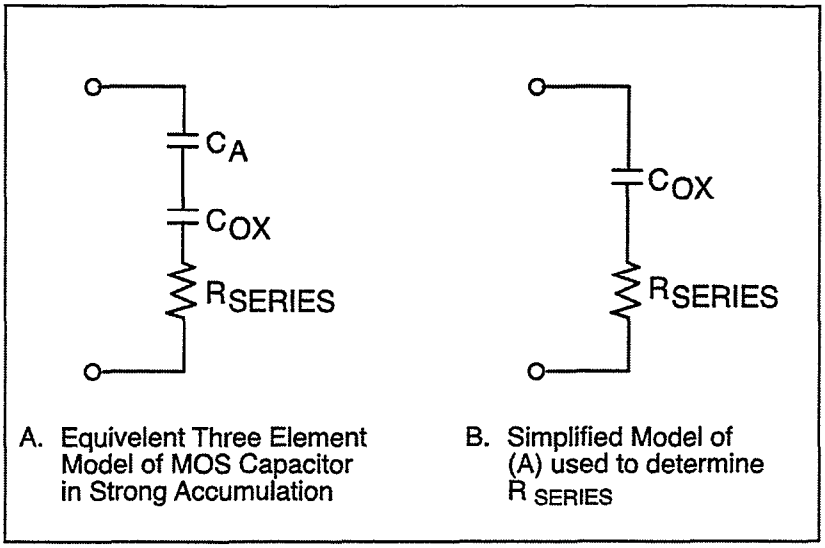


Figure 11 Simplified Model to Determine Series Resistance

From Nicollian and Brews 224, the correction capacitance, C_C, and corrected conductance, G_C, are calculated as follows:

$$C_C = \frac{\left(G_M^2 + \omega^2 C_M^2\right) C_M}{a^2 + \omega^2 C_M^2} \qquad (2)$$

and,

$$G_C = \frac{\left(G_M^2 + \omega^2 C_M^2\right) a}{a^2 + \omega^2 C_M^2} \qquad (3)$$

Where:

$a = G_M - (G^2_M + \omega^2 C^2_M) R_{SERIES}$

C_C = series resistance compensated parallel model capacitance

C_M = measured parallel model capacitance

G_C = series resistance compensated conductance

G_M = measured conductance

R_{SERIES} = series resistance

Gain and offset

Gain and offset can be applied to C_Q and C_H data to allow for curve alignment or to compensate for measurement errors. A gain factor is a multiplier that is applied to all elements of C_Q or C_H array data before plotting or graphics array calculation. Offset is a constant value added to or subtracted from all C_Q and C_H data before plotting or array calculation.

For example, assume that you compare the C_Q and C_H values at reading #3, and you find that C_Q is 2.3pF less than C_H. If you then add an offset of +2.3pF to C_Q, the C_Q and C_H values at reading #3 will then be the same, and the C_Q and C_H curves will be aligned at that point.

Gain and offset values do not affect raw C_Q and C_H values stored in the data file, but the gain and offset values will be stored in the data file so that compensated curves can easily be regenerated at a later date.

Flatband Capacitance and Flatband Voltage

The Model 82-WIN uses the flatband capacitance method of finding flatband voltage, V_{FB}. The Debye length is used to calculate the ideal value of flatband capacitance, C_{FB}. Once the value of C_{FB} is known, the value of V_{FB} is interpolated from the closest V_{GS} values (Nicollian and Brews 487-488).

The method used is invalid when interface trap density becomes very large (10^{12} - 10^{13} and greater). However, this algorithm should give satisfactory results for most users. Those who are dealing with high values of D_{IT} should consult the appropriate literature for a more appropriate method.

Based on doping, the calculation of C_{FB} uses N at 90% W_{MAX}, or user-supplied N_A (bulk doping for p-type, acceptors) or N_D (bulk doping for n-type, donors).

C_{FB} is calculated as follows:

$$C_{FB} = \frac{C_{OX} \in_S A/\left(1\times10^{-4}\right)(\lambda)}{\left(1\times10^{-12}\right)\left(C_{OX}\right)+ \in_S A/\left(1\times10^{-4}\right)(\lambda)} \qquad (4)$$

Where:

C_{FB} = flatband capacitance (pF)

C_{OX} = oxide capacitance (pF)

$\in_S$ = permittivity of substrate material (F/cm)

A = gate area (cm^2)

1×10^{-4} = units conversion for λ

1×10^{-12} = units conversion for C_{OX}

And λ = extrinsic Debye length =

$$\left(1\times10^{4}\right)\left(\frac{\in_S kT}{q^2 N_X}\right)^{1/2} \qquad (5)$$

Where:

kT = thermal energy at room temperature (4.046×10^{-21} J)

q = electron charge (1.60219×10^{-19} coul.)

N_X = N at 90% W_{MAX}, or N_A or N_D when input by the user.

N at 90% W_{MAX} is chosen to represent bulk doping.

Threshold Voltage

The threshold voltage, V_{TH}, is the point on the C-V curve where the surface potential ψ_S, equals twice the bulk potential, ϕ_B. This point on the curve corresponds to the onset of strong inversion. For an enhancement mode MOSFET, V_{TH} corresponds to the point where the device begins to conduct.

V_{TH} is calculated as follows:

(6)

$$V_{TH} = \left[\pm \frac{A}{10^{12} C_{OX}} \sqrt{4 \in_S q \left| N_{BULK} \right| \left| \phi_B \right|} + 2 \left| \phi_B \right| \right] + V_{FB}$$

Where:

V_{TH} = threshold voltage (V)

A = gate area (cm^2)

C_{OX} = oxide capacitance (pF)

10^{12} = units multiplier

$\in_S$ = permittivity of substrate material

q = electron charge (1.60219×10^{-19} coul.)

N_{BULK} = bulk doping (cm^{-3})

ϕ_B = bulk potential (V)

V_{FB} = flatband voltage (V)

Metal Semiconductor Work Function Difference

The metal semiconductor work function difference, W_{MS}, is commonly referred to as the work function. It contributes to the shift in V_{FB} from the ideal zero value, along with the effective oxide charge (Nicollian and Brews 462-477; Sze 395-402). The work function represents the difference in work necessary to remove an electron from the gate and from the substrate, and it is derived as follows:

$$W_{MS} = W_M - \left[W_S + \frac{E_G}{2} - \phi_B \right] \qquad (7)$$

Where:

W_M = metal work function (V)

W_S = substrate material work function (electron affinity) (V)

E_G = substrate material bandgap (V)

ϕ_B = bulk potential (V)

For silicon, silicon dioxide, and aluminum:

$$W_{MS} = 4.1 - \left[4.15 + \frac{1.12}{2} - \phi_B \right] \qquad (8)$$

So that,

$$W_{MS} = -0.61 + \phi_B \qquad (9)$$

$$W_{MS} = -0.61 - \left(\frac{kT}{q} \right) \ln\left(\frac{N_{BULK}}{n_I} \right) (DopeType) \qquad (10)$$

Where, DopeType is +1 for p-type materials, and -1 for n-type materials. For example, for an MOS capacitor with an aluminum gate and p-type silicon ($N_{BULK} = 10^{16}cm^{-3}$), W_{MS} = -0.95V. Also, for the same gate and n-type silicon ($N_{BULK} = 10^{16}cm^{-3}$), W_{MS} = -0.27V.

Effective Oxide Charge

The effective oxide charge, Q_{EFF}, represents the sum of oxide fixed charge, Q_F, mobile ionic charge, Q_M, and oxide trapped charge, Q_{OT}. Q_{EFF} is distinguished from interface trapped charge, Q_{IT}, in that Q_{IT} varies with gate bias and $Q_{EFF} = Q_F + Q_M + Q_{OT}$ does not (Nicollian and Brews 424-429, Sze 390-395). Simple measurements of oxide charge using C-V measurements do not distinguish the three components of Q_{EFF}. These three components can be distinguished from one another by temperature cycling, as discussed in Nicollian and Brews, 429, Fig. 10.2. Also, since the charge profile in the oxide is not known, the quantity, Q_{EFF} should be used as a relative, not absolute measure of charge. It assumes that the charge is located in a sheet at the silicon-silicon dioxide interface. From Nicollian and Brews, Eq. 10.10, we have:

$$V_{FB} - W_{MS} = -\frac{Q_{EFF}}{C_{OX}} \qquad (11)$$

Note that C_{OX} here is per unit of area. So that,

$$Q_{EFF} = \frac{C_{OX}\left(W_{MS} - V_{FB}\right)}{A} \qquad (12)$$

However, since C_{OX} is in F, we must convert to pF by multiplying by 10^{-12} as follows:

$$Q_{EFF} = 10^{-12} \frac{C_{OX}\left(W_{MS} - V_{FB}\right)}{A} \qquad (13)$$

Where:

Q_{EFF} = effective charge (coul/cm^2)

C_{OX} = oxide capacitance (pF)

W_{MS} = metal semiconductor work function (V)

A = gate area (cm^2)

For example, assume a 0.01cm^2 50pF capacitor with a flatband voltage of -5.95V, and a p-type $N_{BULK} = 10^{16}$cm^{-3} (resulting in W_{MS} = -0.95V). In this case, $Q_{EFF} = 2.5 \times 10^{-8}$ coul/cm^2.

The effective oxide charge concentration, N_{EFF}, is computed from effective oxide charge and electron charge as follows:

$$N_{EFF} = \frac{Q_{EFF}}{q} \qquad (14)$$

Where:

N_{EFF} = effective concentration of oxide charge (Units of charge/cm^2)

Q_{EFF} = effective oxide charge (coul./cm^2)

q = electron charge (1.60219×10^{-19} coul.)

For example, with an effective oxide charge of 2.5×10^{-8} coul/cm^2, the effective oxide charge concentration is:

$$N_{EFF} = \frac{2.5 \times 10^{-8}}{1.60219 \times 10^{-19}} \qquad (15)$$

$$N_{EFF} = 1.56 \times 10^{11}\, units / cm^2 \qquad (16)$$

Doping Profile

Depletion Depth vs. Gate Voltage (V_{GS})

Model 82-WIN computes the depletion depth, w, from the high-frequency capacitance and oxide capacitance at each measured value of V_{GS} (Nicollian and Brews 386). In order to graph this function, the program computes each w element of the calculated data array as shown below.

$$w = A \in_S \left(\frac{1}{C_H} - \frac{1}{C_{OX}} \right) \qquad (17)$$

Where:

w = depth (μm)

$\in_S$ = permittivity of substrate material

C_H = high-frequency capacitance (pF)

C_{OX} = oxide capacitance (pF)

A = gate area (cm^2)

$1/C_H^2$ vs. Gate Voltage

A $1/C^2$ graph can yield important information about doping profile. N is related to the reciprocal of the slope of the $1/C^2$ vs. V_{GS} curve, and the V intercept point is equal to the flatband voltage caused by surface charge and metal-semiconductor work function (Nicollian and Brews 385).

Doping Concentration vs. Depth

The doping profile of the device is derived from the C-V curve based on the definition of the differential capacitance (measured by the Models 590 and 595) as the differential change in

depletion region charge produced by a differential change in gate voltage (Nicollian and Brews 380-389).

The standard N vs. w analysis discussed here does not compensate for the onset of accumulation, and it is accurate only in depletion. This method becomes inaccurate when the depth is less than two Debye lengths.

In order to correct for errors caused by interface traps, the error term $(1-C_Q/C_{OX})/(1-C_H/C_{OX})$ is included in the calculations as follows:

(18)

$$N = \frac{\left(-2\times10^{-24}\right)\left[\left(1-C_Q/C_{OX}\right)/\left(1-C_H/C_{OX}\right)\right]}{A^2 q\,\epsilon_S}\left[\frac{d}{dV_{GS}}\left(\frac{1}{C_H^2}\right)\right]^{-1}$$

Where:

N = doping concentration (cm^{-3})

C_Q = quasistatic capacitance (pF)

C_{OX} = oxide capacitance (pF)

$(1-C_Q/C_{OX})/1-C_H/C_{OX})$ = voltage stretchout term

C_H = high-frequency capacitance (pF)

A = gate area (cm^2)

q = electron charge (1.60219×10^{-19} coul.)

ϵ_S = permittivity of substrate material

1×10^{-24} = units conversion factor

Band Bending (ψ_S) vs. Gate Voltage

As a preliminary step, surface potential (ψ_S - ψ_0) vs. V_{GS} is calculated with the results placed in the ψ_S column of the array. Surface potential is calculated as follows:

$$\left(\psi_S - \psi_0\right) = \sum_{V_{GS}\#1}^{V_{GS}Last} \left(1 - C_Q / C_{OX}\right)\left(2V_{STEP}\right) \qquad (19)$$

Where:

(ψ_S - ψ_0) = surface potential (V)

C_Q = quasistatic capacitance (pF)

C_{OX} = oxide capacitance (pF)

V_{STEP} = step voltage (V)

V_{GS} = gate-substrate voltage (V)

Note that the (ψ_S - ψ_0) value is accumulated as the column is built, from the first row of the array (V_{GS} #1) to the last array row (V_{GS} last). The number of rows will, of course, depend on the number of readings in the sweep, which is determined by the Start, Stop and Step voltages.

Once (ψ_S - ψ_0) values are stored in the array, the value of (ψ_S - ψ_0) at the flatband voltage is used as a reference point and is set zero by subtracting that value from each entry in the (ψ_S - ψ_0) column, changing each element in the column to ψ_S.

Interface Trap Capacitance C_{IT} and Density D_{IT}

Interface trap density is calculated from C_{IT} as shown below (Nicollian and Brews 322).

$$C_{IT} = \left(\frac{1}{C_Q} - \frac{1}{C_{OX}}\right)^{-1} - \left(\frac{1}{C_H} - \frac{1}{C_{OX}}\right)^{-1} \qquad (20)$$

And,

$$D_{IT} = \frac{\left(1 \times 10^{-12}\right) C_{IT}}{A} \qquad (21)$$

Where:

C_{IT} = interface trap capacitance (pF)

D_{IT} = interface trap density ($cm^{-2}\ eV^{-1}$)

C_Q = quasistatic capacitance (pF)

C_H = high-frequency capacitance (pF)

C_{OX} = oxide capacitance (pF)

A = gate area (cm^2)

q = electron charge (1.60219×10^{-19}coul.)

1×10^{-12} = units conversion for C_{IT}

Mobile Ion Monitoring with Triangular Voltage Sweep (STVS) Method

STVS is a new technique developed by Keithley to monitor mobile ion charge in MOS structures. Compared with other mobile ion monitoring techniques, such as the BTS and flatband shift methods, it offers faster and more accurate measurement. STVS measures ionic current instead of voltage shift. It has the ability to identify species, and it eliminates the need for temperature cycling of the Device Under Test (DUT). The STVS method has proven to be effective in monitoring mobile ion charge in dielectrics to levels down to $10^9 cm^{-3}$.

The STVS library can perform the corresponding mobile ion charge analysis. It has a built-in correction algorithm to eliminate the problems associated with leakage current. Many parameters, including mobile ion charge concentration, can be extracted from this measurement.

The STVS method improves on the conventional TVS method (discussed below) by measuring both C_Q and C_H and then computing mobile ion charge concentration as follows:

$$N_M = \frac{\sum_{-V_{GS}}^{+V_{GS}} \left(C_Q - C_H\right) \Delta V_{GS}}{q} \qquad (22)$$

Where:

N_M = mobile ion density ($1/cm^3$)

V_{GS} = gate-substrate voltage (V)

ΔV_{GS} = change in gate-substrate voltage (step voltage) (V)

C_Q = quasistatic capacitance measured by Model 595 (F)

C_H = high-frequency capacitance measured by Model 590 (F)

q = electron charge (coul.)

Flatband Voltage Shift Method

The primary method for measuring oxide charge density is the flatband voltage shift or temperature-bias stress method (Snow et al). In this case, two high-frequency C-V curves are measured, both at room temperature. Between the two curves, the device is biased with a voltage at 200-300°C to drift mobile ions across the oxide. The flatband voltage differential between the two curves is then calculated, from which charge density can be determined.

From Nicollian and Brews (426, Eq. 10.9 and 10.10), we have:

$$V_{FB} - W_{MS} = \frac{\bar{x}Q_O}{\epsilon_{OX}} = \frac{\bar{x}Q_O}{X_O C_{OX}} \qquad (23)$$

Where:

$\bar{x}Q_O$ = the first moment of the charge distribution

$\bar{x}$ = charge centroid

W_{MS} = metal semiconductor work function (constant)

ϵ_{OX} = oxide dielectric constant

X_o = oxide thickness

C_{OX} = oxide capacitance

So that:

$$\Delta V_{FB} = \Delta\left(V_{FB} - W_{MS}\right) \qquad (24)$$

$$\Delta V_{FB} = \Delta \frac{\bar{x}Q_O}{\epsilon_{OX}} \qquad (25)$$

$$\Delta V_{FB} = \frac{Q_O}{C_{OX}} \Delta \frac{\bar{x}}{X_O} \qquad (26)$$

For the common case of thermally grown oxide, $\bar{x}$ (before) = X_O and $\bar{x}$ (after) = 0, so that

$$\Delta V_{FB} = \frac{-Q_o}{C_{OX}} \qquad (27)$$

Where Q_O is the effective charge. Divide Q_O by the gate area to obtain mobile ion charge density per unit area.

Triangular Voltage Sweep (TVS) Method

Yet another way to measure oxide charge density is the triangular voltage sweep (TVS) method (Nicollian and Brews 435-440).

Although the method presented here was originally developed for the ramp technique of quasistatic measurement, the Model 595 is used to make the necessary measurement. The end result is the same: the area between the measured capacitance curve and C_{OX} indicates the charge density as follows:

$$\sum_{-V_{GS}}^{+V_{GS}} \left(C_{MEAS} - C_{OX}\right) \Delta V_{GS} = qN_M \left[\frac{\bar{x}\left(V_{GS}\right)}{X_O} - \frac{\bar{x}\left(-V_{GS}\right)}{X_O} \right] \qquad (28)$$

Where:

V_{GS} = gate-substrate voltage (V)

ΔV_{GS} = change in gate-substrate voltage (step voltage) (V)

C_{MEAS} = quasistatic capacitance measured by Model 595 (F)

C_{OX} = oxide capacitance (F)

q = electron charge (coul.)

N_M = mobile ion density ($1/cm^3$)

$\overline{X}$ = charge centroid

X_O = oxide thickness (m)

Q_O = mobile ion charge (coul.)

or, in the case of thermally grown oxide, the above reduces to:

$$\sum_{-V_{GS}}^{+V_{GS}} \left(C_{MEAS} - C_{OX}\right) \Delta V_{GS} = -Q_O \qquad (29)$$

Generation Velocity and Generation Lifetime (Zerbst Plot)

Zerbst Plot

Zerbst analysis requires two types of data: C-V and C-t. Important data taken from the C-V measurement includes C_{OX}, C_{MIN}, and doping concentration (N_{AVG} and N_{BULK}). The results of the C-V analysis are integrated with data taken during a C-t measurement to compute generation velocity and generation lifetime of electron-hole pairs. These two parameters are computed from the slope and y-axis intercept of the graph of G/n_I vs. $w\text{-}w_F$ as outlined below.

G/n_I Computation

$$G / n_I = -\epsilon_S \, A N_{AVG} C_{OX} \bullet \left[\frac{\frac{1}{C^2_{t(i+1)}} - \frac{1}{C^2_{t(i-1)}}}{n_I t_{int}} \right] \bullet \left(\frac{1 \times 10^{12}}{2} \right) \qquad (30)$$

Where:

G = generation rate (s^{-1})

ϵ_S = permittivity of semiconductor (F/cm)

A = gate area (cm^2)

N_{AVG} = average doping concentration (cm^{-3})

C_{OX} = oxide (maximum) capacitance (pF)

$C_{t(i+1)}$ = (i+1) value of measured C-t capacitance (pF)

$C_{t(i-1)}$ = (i-1) value of measured C-t capacitance (pF)

n_I = intrinsic carrier concentration (cm^{-3})

t_{int} = time interval between C-t measurements (s)

i = [2, #Rdgs-1]

w - w_F Computation

$$w - w_F = 1 \times 10^{12} \epsilon_S A\left(\frac{1}{C_{ti}} - \frac{1}{C_{OX}}\right) - w_F \qquad (31)$$

$$w_F = 1 \times 10^{12} \epsilon_S A\left(\frac{1}{C_{ti}} - \frac{1}{C_{OX}}\right) \qquad (32)$$

Where:

w = depletion depth (cm)

w_F = equilibrium inversion depth (cm)

ϵ_S = permittivity of semiconductor (F/cm)

A = gate area (cm^2)

C_{ti} = i(th) value of measured C-t capacitance (pF)

C_{MIN} = equilibrium minimum capacitance (pF)

Determining Generation Velocity and Generation Lifetime

The generation lifetime, τ_G, is equal to the reciprocal of the slope of the linear portion of the Zerbst plot, while the

generation velocity, s, is the y-axis (G/n_I) intercept of the same linear section of the Zerbst plot.

Constants, Symbols, and Equations Used for Analysis

In order to perform correct analysis, it may be necessary for you to verify or modify the analysis constants to suit your particular device. Before making measurements, it is strongly recommended that you verify that constants are correct to ensure that your analysis is performed correctly. Otherwise, your analysis results will be meaningless.

Default Material Constants

Table 1 lists default material constants, values, descriptions, and symbols used in the libraries.

Table 1 Default Material Constants

Symbol	Description	Default Value
q	Electron charge (Coul.)	1.60219×10^{-19} Coul.
k	Boltzmann's constant (J/°K)	1.38066×10^{-23} J/°K
T	Test temperature (°K)	293°K
ϵ_{OX}	Permittivity of oxide (F/cm)	3.4×10^{-13} F/cm
ϵ_S	Semiconductor permittivity (F/cm)	1.04×10^{-12} F/cm
E_G	Semiconductor energy gap (eV)	1.12eV
n_I	Intrinsic carrier concentration ($1/cm^3$)	1.45×10^{10} cm^{-3}
W_{MS}	Metal work function (V)	4.1V
	Electron affinity (V)	4.15V

Modifying Constants

Constants may be modified as outlined below. For detailed procedures, refer to the Metrics ICS manual.

1. Open the **Transform Editor**.

2. Click on the **Edit Constants** button, and note that a constants window will appear.

3. Scroll down the list of constants, then select the constant you wish to change.

4. Type in the new value, then click on the **STORE** button.

5. Repeat as necessary for other constants. Note that new values will be updated once you exit from this menu.

6. You may add more constants to be used in analysis. Simply type the name, value, and units, then click on the **STORE** button to save them.

Data Symbols

Table 2 summarizes data symbols used in the library along with a description of each symbol. For information on implementation in Keithley libraries, refer to the text file EQUATION.TXT located on the C-V library disk.

Table 2 Data Symbols

Symbol	Description	Units
A	Device gate area.	cm^2
C_{FB}	Flatband capacitance, corresponding to no band bending.	pF
C_H	High-frequency capacitance, as measured by the Model 590 at either 100kHz or1MHz.	pF
C_{HADJ}	The high-frequency capacitance that is adjusted according to gain and offset values. C_{HADJ} is the value that is actually plotted and printed.	pF
C_Q	Quasistatic capacitance as measured by Model 590.	pF
C_{QADJ}	The quasistatic capacitance that is adjusted according to gain and offset values. C_{QADJ} is the value that is actually plotted and printed.	pF
C_Q'	Interpolated value of C_Q set to correspond to the quasistatic capacitance at V.	pF
C_{MIN}	Minimum high-frequency capacitance in inversion.	pF
C_{OX}	Oxide capacitance, usually set to the maximum C_H in accumulation.	pF
D_{IT}	Density or concentration of interface states.	$1/cm^2/eV$
E_C	Energy of conduction band edge (valence band is E_V).	eV
E_T	Interface trap energy.	eV
G	High-frequency conductance, as measured by the Model 590 at either 100kHz or1MHz.	S
N_A	Bulk doping for p-type (acceptors).	$1/cm^3$
N_D	Bulk doping for n-type (donors).	$1/cm^3$
N_{AVG}	Average doping concentration.	$1/cm^3$
N_{BULK}	Bulk doping concentration.	$1/cm^3$
N_{EFF}	Effective oxide charge concentration.	$1/cm^2$
$N(90\% W_{MAX})$	Doping corresponding to 90% maximum w profile (approximates doping in the bulk).	$1/cm^3$
N_M	Mobile ion concentration in the oxide.	$1/cm^3$
Q_{EFF}	Effective oxide charge.	$coul/cm^2$
Q/t	Current measured by the Model 595 at the end of each capacitance measurement with the unit in the capacitance function.	A

Table 2 Data Symbols (continued)

Symbol	Description	Units
R_{SERIES}	Series resistance.	Ω
t_{OX}	Oxide thickness.	nm
V_{GS}	Gate voltage. More specifically, the voltage at the gate with respect to the substrate.	V
V_{FB}	Flatband voltage, or the value of V_{GS} that results in C_{FB}.	V
V_H	Voltage reading sent by Model 590 with matching C_H and G.	V
V_{TH}	The point where the surface potential, ψ_S, is equal to twice the bulk potential, ϕ_B.	V
w	Depletion depth or thickness. Silicon under the gate is depleted of minority carriers in inversion and depletion.	μm
ψ_S	Silicon surface potential as a function of V_{GS}. More precisely, this value represents band bending and is related to surface potential via the bulk potential.	V
ψ_0	Offset in ψ_S due to calculation method and V_0.	V
ϕ_B	Silicon bulk potential.	V
λ	Extrinsic Debye length.	m

Summary of Analysis Equations

Table 3 summarizes analysis equations used by the Model 82-WIN software. Refer to earlier sections of this chapter for more details on these equations.

Table 3 Analysis Equations

Analysis Function	Equation
Band Bending	$\left(\psi_S - \psi_0\right) = \sum_{V_{GS}\#1}^{V_{GS}Last} \left(1 - C_Q / C_{OX}\right)\left(2V_{STEP}\right)$
Depletion Depth	$w = A \in_S \left(\frac{1}{C_H} - \frac{1}{C_{OX}}\right)$
Doping Concentration	$N = \frac{\left(-2\times10^{-24}\right)\left[\left(1 - C_Q / C_{OX}\right)/\left(1 - C_H / C_{OX}\right)\right]}{A^2 q \in_S}\left[\frac{d}{dV_{GS}}\left(\frac{1}{C_H^2}\right)\right]^{-1}$
Effective Oxide Charge	$Q_{EFF} = \frac{C_{OX}\left(W_{MS} - V_{FB}\right)}{A}$
Effective Charge Concentration	$N_{EFF} = \frac{Q_{EFF}}{q}$
Flatband Capacitance	$C_{FB} = \frac{C_{OX} \in_S A/\left(1\times10^{-4}\right)(\lambda)}{\left(1\times10^{-12}\right)\left(C_{OX}\right) + \in_S A/\left(1\times10^{-4}\right)(\lambda)}$ Where: $\lambda = \left(1\times10^{4}\right)\left(\frac{\in_S kT}{q^2 N_x}\right)^{1/2}$ And N_X =N at 90% W_{MAX}, N_A, or N_D

Table 3 Analysis Equations (continued)

Analysis Function	Equation
Flatband Voltage Shift	$V_{FB} - W_{MS} = \frac{\bar{x}Q_O}{\epsilon_{OX}} = \frac{\bar{x}Q_O}{X_O C_{OX}}$ $\Delta V_{FB} = \frac{-Q_O}{C_{OX}}$
Interface Trap Capacitance Interface Trap Density	$C_{IT} = \left(\frac{1}{C_Q} - \frac{1}{C_{OX}}\right)^{-1} - \left(\frac{1}{C_H} - \frac{1}{C_{OX}}\right)^{-1}$ $D_{IT} = \frac{\left(1\times 10^{-12}\right)C_{IT}}{A}$
Mobile Ion Charge Concentration TVS Method STVS Method	$\sum_{-V_{GS}}^{+V_{GS}} \left(C_{MEAS} - C_{OX}\right)\Delta V_{GS} = -Q_O$ $N_M = \frac{\sum_{-V_{GS}}^{+V_{GS}} \left(C_Q - C_H\right)\Delta V_{GS}}{q}$
Oxide Thickness/Gate Area	$t_{OX} = \frac{A\,\epsilon_{OX}}{\left(1\times 10^{-19}\right)C_{OX}}$

Table 3 Analysis Equations (continued)

Analysis Function	Equation
Series Resistance Compensation	$C_C = \frac{\left(G_M^2 + \omega^2 C_M^2\right) C_M}{a^2 + \omega^2 C_M^2}$ $G_C = \frac{\left(G_M^2 + \omega^2 C_M^2\right) a}{a^2 + \omega^2 C_M^2}$ $a = G_M - \left(G_M^2 + \omega^2 C_M^2\right) R_{SERIES}$
Threshold Voltage	$V_{THRESHOLD} = \left[\pm \frac{A}{10^{12} C_{OX}} \sqrt{4 \in_S q \left\| N_{BULK} \right\| \phi_B \| + 2 \left\| \phi_B \right\|} \right] + V_{FB}$
Work Function	$W_{MS} = W_M - \left[W_S + \frac{E_G}{2} - \phi_B \right]$
Zerbst Plot (Generation Lifetime and Velocity)	$G / n_i = - \in_S AN_{AVG} C_{OX} \bullet \left[\frac{\frac{1}{C^2_{t(i+1)}} - \frac{1}{C^2_{t(i-1)}}}{n_i t_{int}} \right] \bullet \left(\frac{1 \times 10^{12}}{2} \right)$ $w - w_F = 1 \times 10^{12} \in_S A \left(\frac{1}{C_{ti}} - \frac{1}{C_{OX}} \right) - w_F$

References and Bibliography of C-V Measurements

References

The references below are cited in this chapter.

Nicollian, E.H. and Brews, J.R., MOS Physics and Technology. Wiley, New York (1982).

Sze, S.M., Physics of Semiconductor Devices 2nd edition. Wiley, New York (1985)

Snow, E.H. Grove, A.S., Deal, B.E., and Sah, C.T. J., "Ionic Transport Phenomena in Insulating Films", Appl. Phys., 36, 1664 (1965)

Bibliography of C-V Measurements

Texts

Grove, A.S., Physics and Technology of Semiconductor Devices. Wiley, New York (1967).

Sze, S.M., Semiconductor Devices. Physics and Technology. Wiley, New York (1985).

Articles and Papers

Feedback Charge Method

Mego, T.J. `"Improved Feedback Charge Method for Quasistatic CV Measurements in Semiconductors". Rev. Sci. Instr. 57, 11 (1986).

Mego, T.J. "Improved Quasistatic CV Measurement Method for MOS". Solid State Technology, 29, 11, 519-21 (1986).

Markgraf, W., Baumann, M., Beyer, A., Arst, P., Rennau, M., "Nutzung der statischen CU-Methode im Ranen eines mikrorechnergesteuerten MOS-Messplatzes", Phys. d. Halbleiteroberflaeche. 15, 73 (1984).

Q-V Static Method

Ziegler, K. and Klausmann, E., "Static Technique for Precise Measurements of Surface Potential and Interface State Density in MOS Structures", Appl. Phys. Lett. 26, 400 (1975).

Kirov, K., Alexsandrova, S., and Minchev, c., "Error in Surface State Determination Caused by Numerical Differentiation of Q-V Data", Solid State Electronics. 18, 341(1978).

Q-C Method and Simultaneous High-low Frequency C-V

Nicollian, E.H. and Brews, J.R., "Instrumentation and Analog Implementation of the Q-C Method for MOS Mesurements", Solid State Electronics. 27, 953 (1984).

Boulin, D.M., Brews, J.R., and Nicollian, E.H., "Digital implementation of the Q-C Method for MOS Measurements", Solid State Electronics. 27, 977 (1984).

Derbenwick, G.F., "Automated C-V and |Y|-w Curves for MOS Device Analysis", Sandia Report SAND80-1308 (1982).

Lubzens, D., Kolodny, A., and Shacham-Diamond, Y.J., "Automated Measurement and Analysis of MIS Interfaces in

Narrow-Bandgap Semiconductors," IEEE transactions on Electron Devices, ED-28, 5 (1981).

Ramp Method

Kuhn, M., "A Quasistatic Technique for MOS C-V and Surface State Measurements", Solid State Electronics. 13, 873 (1970).

Castagne, R., "Détermination de la densité d'états lents d'une capacité métak-isolant semiconducteur par l'étude de la charge sous une tension croissant line áirement", C.R.Acad. Sci. 267, 866 (1968).

Kerr, D.R., "MIS Measurement Technique Utilizating Slow Voltage Ramps", Int.Conf. Properties and Use of MIS Structures, Grenoble, France, 303 (1969).

Castagne, R, and Vapaille, A., "Description of the SiO_2-Si Interface Properties by Means of Very Low Frequency MOS Capacitance Measurements", Surface Science, 28, 157 (1971).

Kuhn, M. and Nicollian, E.H., "Nonequilibrium Effects in Quasi-static MOS Measurements", J. Electrochem.Soc., 118, 373 (1971).

Lopez A.D., "Using the Quasistatic Method for MOS Measurements", Rev.Sci.Instr. 44, 200 (1973).

Interface States/Doping Profiles

Berglund, C.N., "Surface States at Steam Grown Silicon-Silicon Dioxide Interfaces", IEEE Trans.Electron.Dev., 13, 701 (1966).

DeClerck, G., "Characterization of Surface States at the Si-SO2 Interface", Nondestructive Evaluation of Semiconductor Materials and Devices (J.N. Zemel, ed.) Plenum Press, New York, p. 105 (1979).

Brews, J.R., "Correcting Interface-State Errors in MOS Doping Profile Determinations", J.Appl. Phys. 44, 3228 (1973).

Gordon, B.J., "On-Line Capacitance-Voltage Doping Profile Measurement of Low-Dose Ion implants", IEEE Trans. Dev., ED-27, 12 (1980).

VanGelder, W., and Nicollian, E.H., "Silicon Impurity Distribution as Revealed by Pulsed MOS C-V Measurements, "J. Electrochem, Soc. Solid State Science, 118, 1(1971).

MOS Process Characterization

Zaihinger, K.H. and Heiman, F.P., "The C-V Technique as an Analytical Tool", Solid State Technology. 13:5-6 (1970).

McMillian, L., "MOS C-V Techniques for IC Process Control", Solid State Technology. 15, 47 (1972).

Zerbst, M., "Relaxationseffekte an Halbeiter Isolator-Grenzflaechen", Z.Angnew.Phys. 22, 30 (1966).

Mobile Ion Charge Monitoring

Stauffer, L., et al., "Mobile Ion Monitoring by Simultaneous Triangular Voltage Sweep", Solid State Technology. 38, S3 (1995).

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Name and Telephone No. _____

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List all control settings, describe problem and check boxes that apply to problem. _____

_____

_____

❑ Intermittent ❑ Analog output follows display ❑ Particular range or function bad; specify

_____

❑ IEEE failure ❑ Obvious problem on power-up ❑ Batteries and fuses are OK

❑ Front panel operational ❑ All ranges or functions are bad ❑ Checked all cables

Display or output (check one)

❑ Drifts ❑ Unable to zero ❑ Unstable

❑ Overload ❑ Will not read applied input

❑ Calibration only ❑ Certificate of calibration required ❑ Data required

(attach any additional sheets as necessary)

Show a block diagram of your measurement including all instruments connected (whether power is turned on or not). Also, describe signal source.

Where is the measurement being performed? (factory, controlled laboratory, out-of-doors, etc.)_____

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What power line voltage is used?_____ Ambient temperature?_____°F

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Any additional information. (If special modifications have been made by the user, please describe.)

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